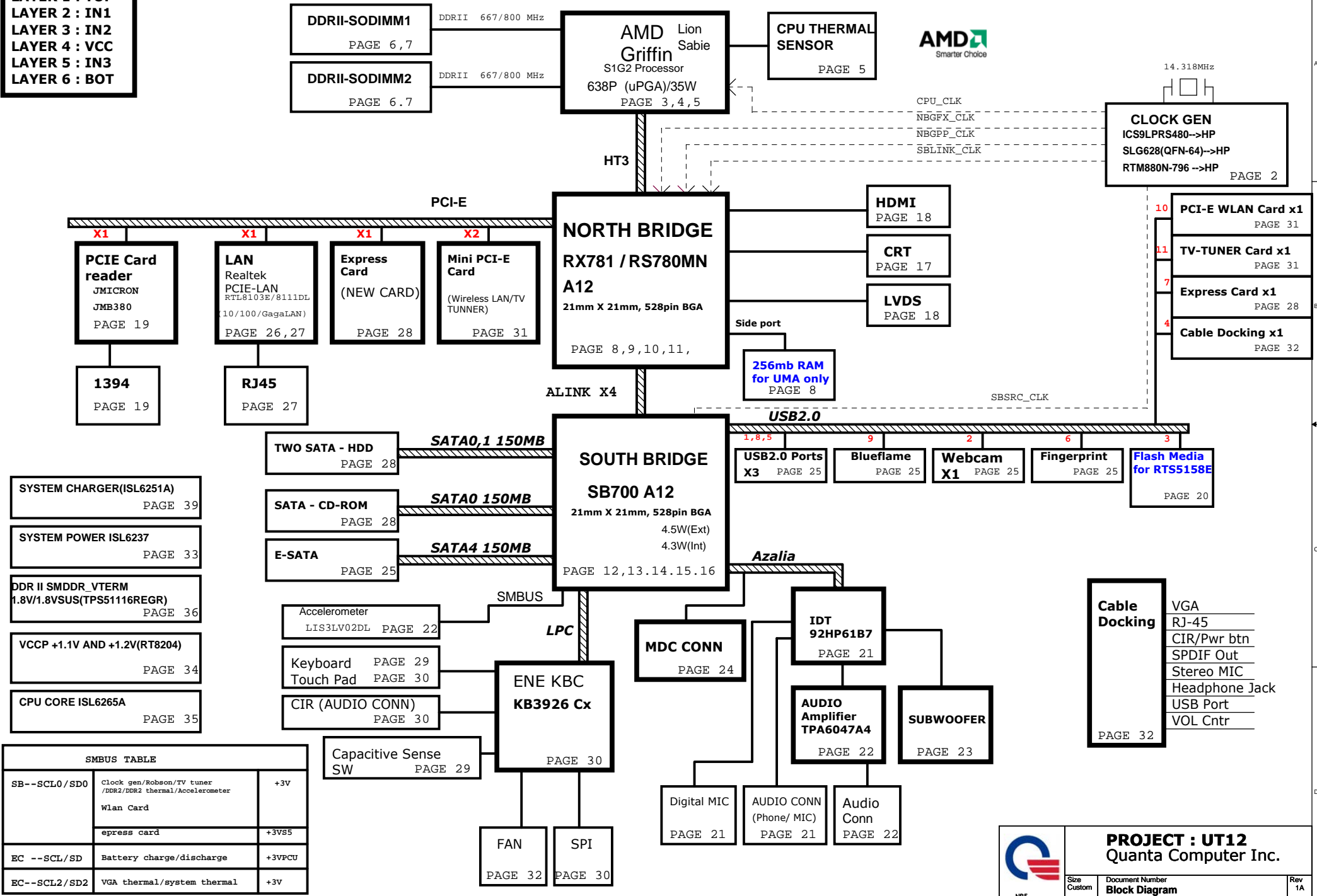
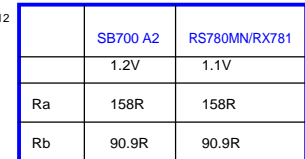
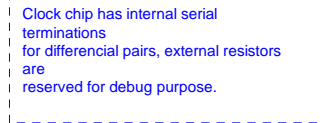


# UT12(UMA) SYSTEM DIAGRAM


**PCB STACK UP**  
LAYER 1 : TOP  
LAYER 2 : IN1  
LAYER 3 : IN2  
LAYER 4 : VCC  
LAYER 5 : IN3  
LAYER 6 : BOT

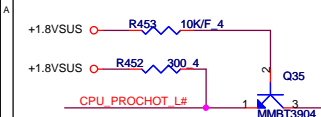
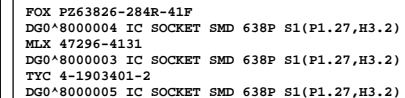


SMBUS TABLE		
SB--SCL0/SD0	Clock gen/Robson/TV tuner /DDR2/DDR2 thermal/Accelerometer	+3V
	Wlan Card	
	epress card	+3VS5
EC --SCL/SD	Battery charge/discharge	+3VPCU
EC--SCL2/SD2	VGA thermal/system thermal	+3V

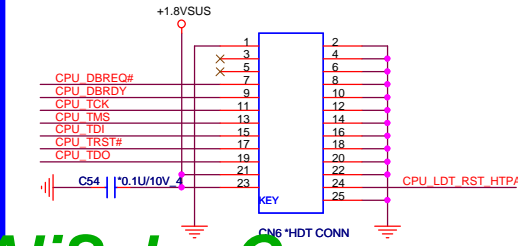


RES CHIP 130 1/16W +1%(0402)L-F -->CS11302FB15  
RES CHIP 158 1/16W +1%(0402) -->CS11582FB00  
RES CHIP 90.9 1/16W +1%(0402) -->CS09092FB15  
RES CHIP 82.5 1/16W +1%(0402) -->CS08252FB11

 NB5	<b>PROJECT : UT12</b> Quanta Computer Inc.		
	Size Custom	Document Number <b>Clock Generator</b>	Rev 1A
	Date: Monday, November 10, 2008    Sheet   2    of   40		

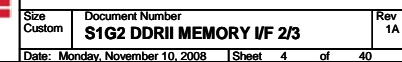


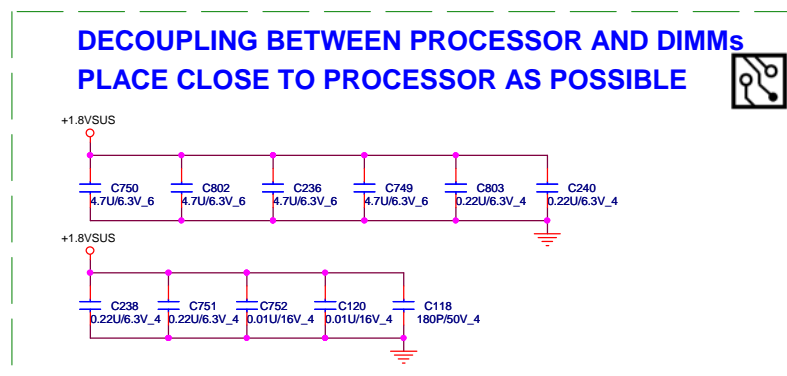
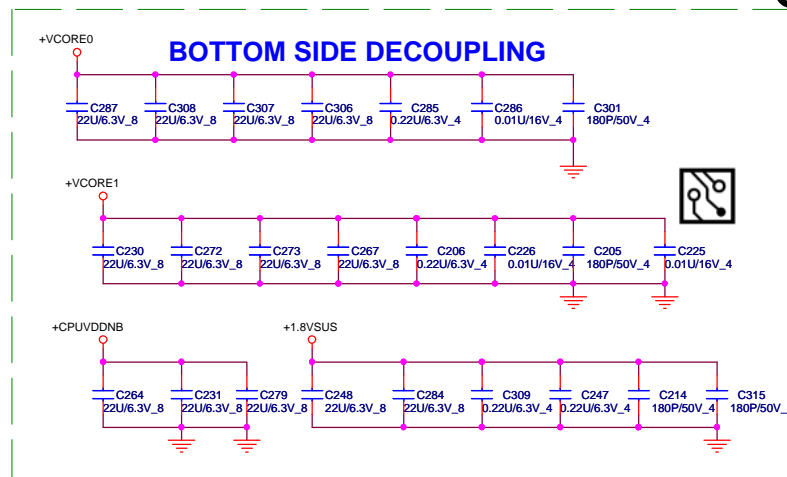
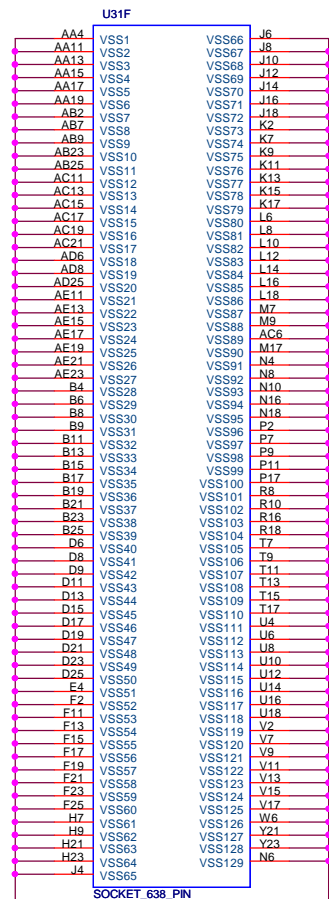
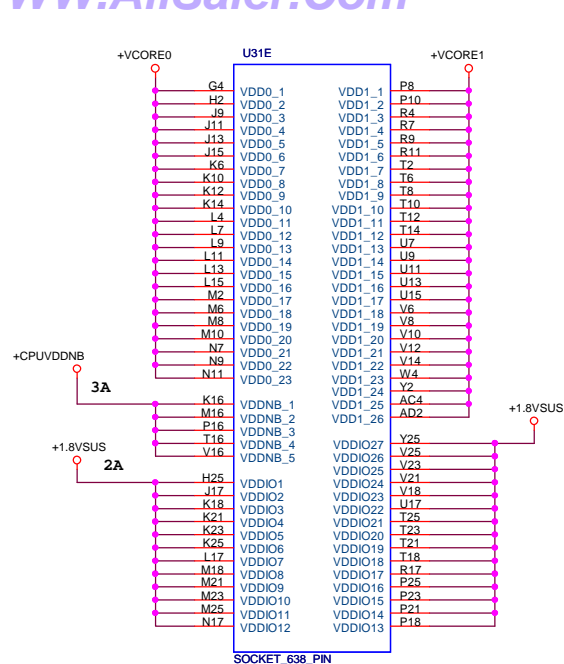
## HDT Connector



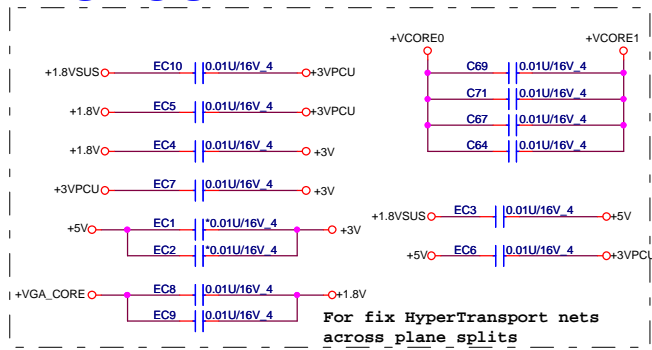
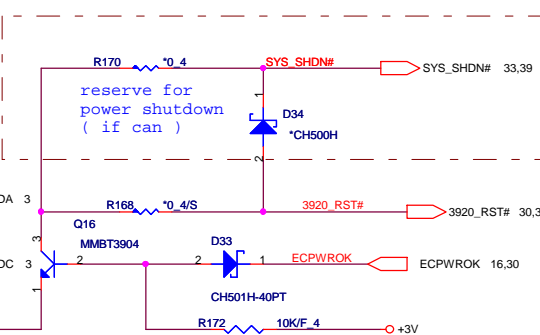
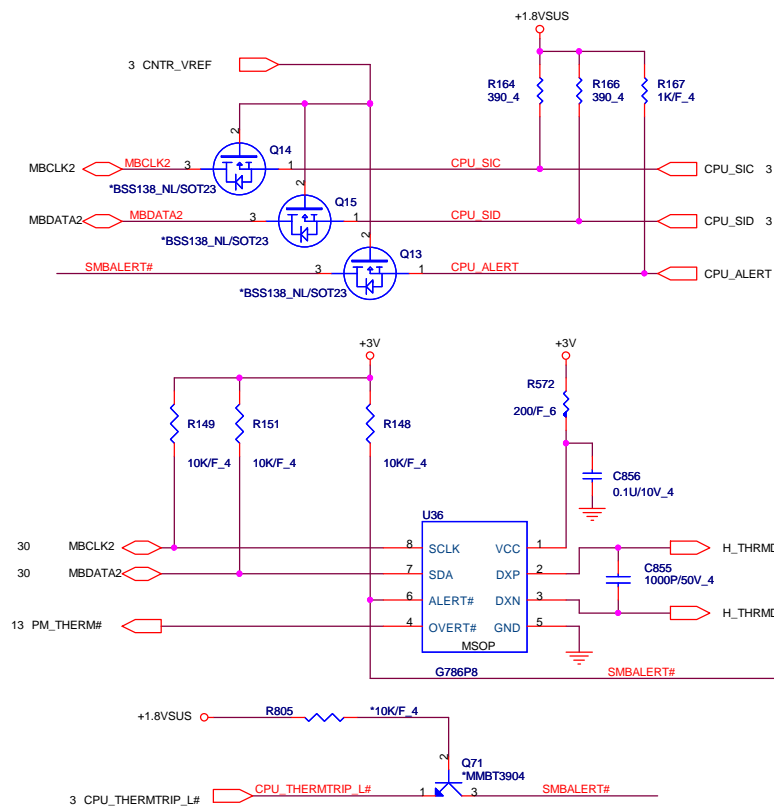
SVC	SVD	Voltage Output
0	0	1.4V
0	1	1.2V
1	0	1.0V
1	1	0.8V

**PROJECT : UT12**  
Quanta Computer Inc.





## PROCESSOR POWER AND GROUND

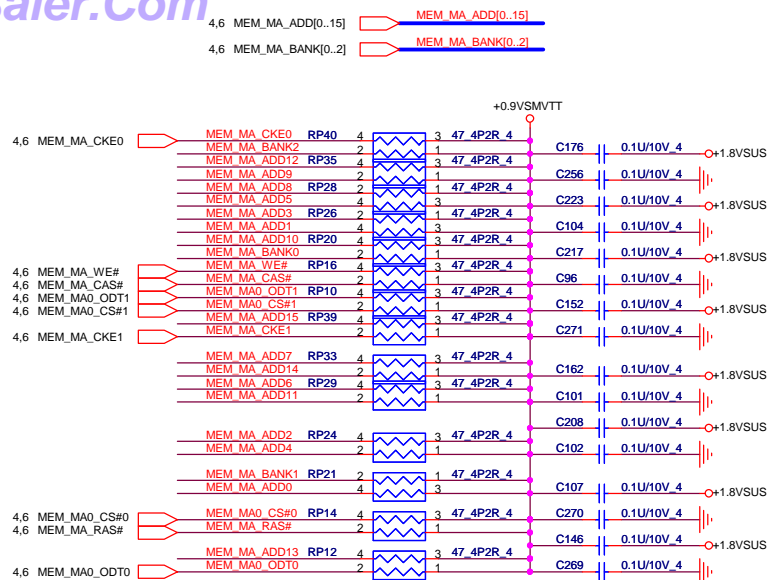


**PROJECT : UT12**  
Quanta Computer Inc.

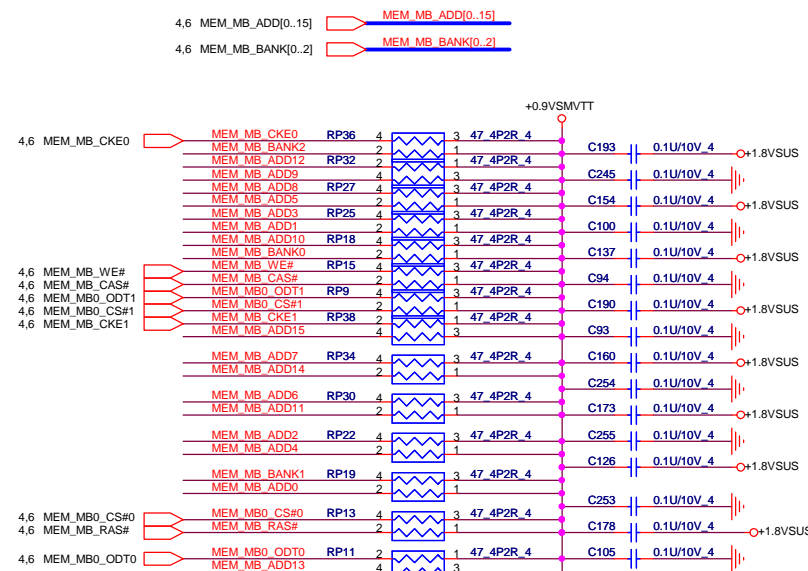
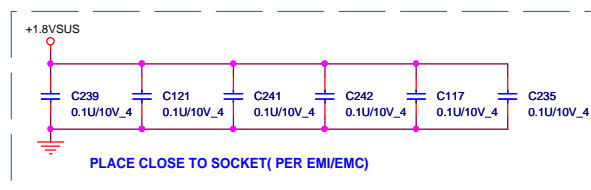
Size Custom	Document Number S1G2 PWR & GND 3/3	Rev 1A
Date: Monday, November 10, 2008	Sheet 5 of 40	



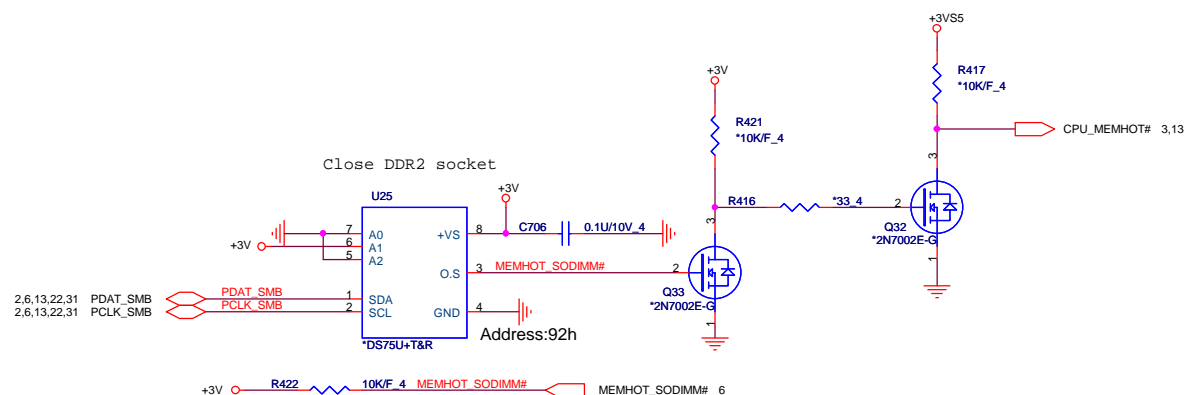
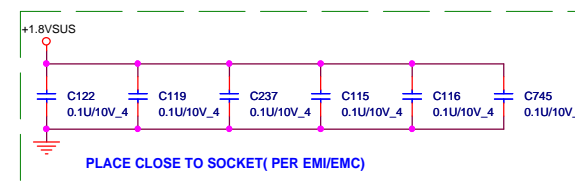




PLACE CLOSE TO PROCESSOR  
WITHIN 1.5 INCH

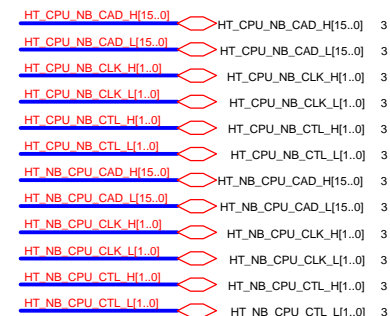


PLACE CLOSE TO PROCESSOR  
WITHIN 1.5 INCH



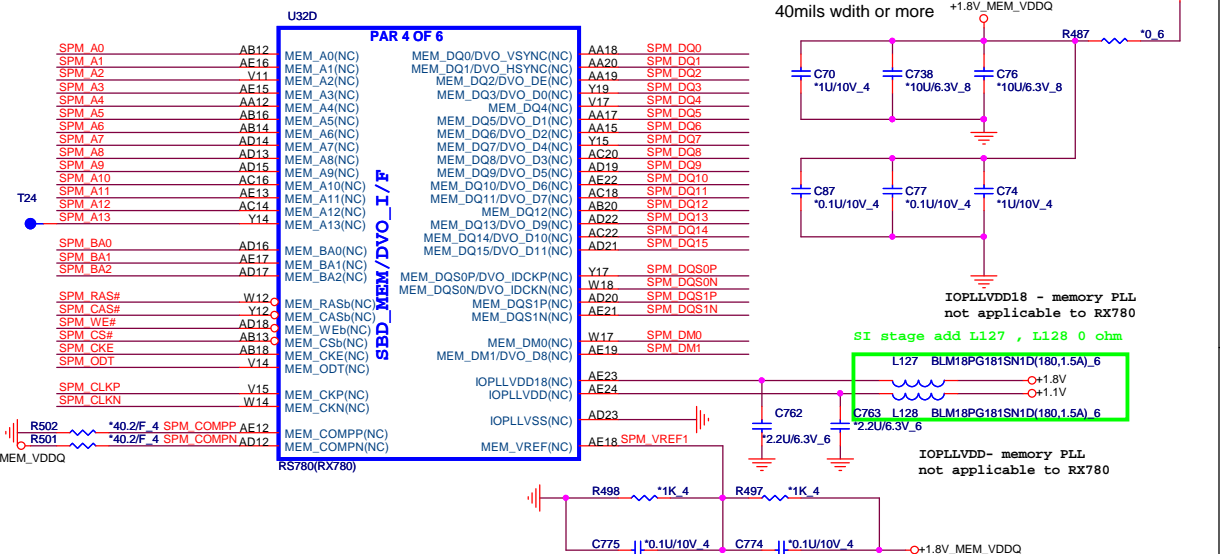
**PROJECT : UT12**  
Quanta Computer Inc.

Size Custom	Document Number	Rev 1A
DDR2 SODIMMS TERMINATIONS		
Date: Monday, November 10, 2008	Sheet 7 of 40	



signals	RS780	RX780
HT_TXCALP	R641 301 ohm 1%	R641 1.21k ohm 1%
HT_TXCALN		
HT_RXCALP	R655 301 ohm 1%	R655 1.21k ohm 1%
HT_RXCALN		

RES CHIP 301 1/16W +-1%(0402)  
P/N : CS13012FB14

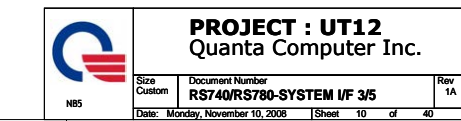


**PROJECT : UT12**  
Quanta Computer Inc.

Size Custom	Document Number <b>RS740/RS780-HT LINK I/F 1/5</b>	Rev 1A
Date: Monday, November 10, 2008		Sheet 8 of 40

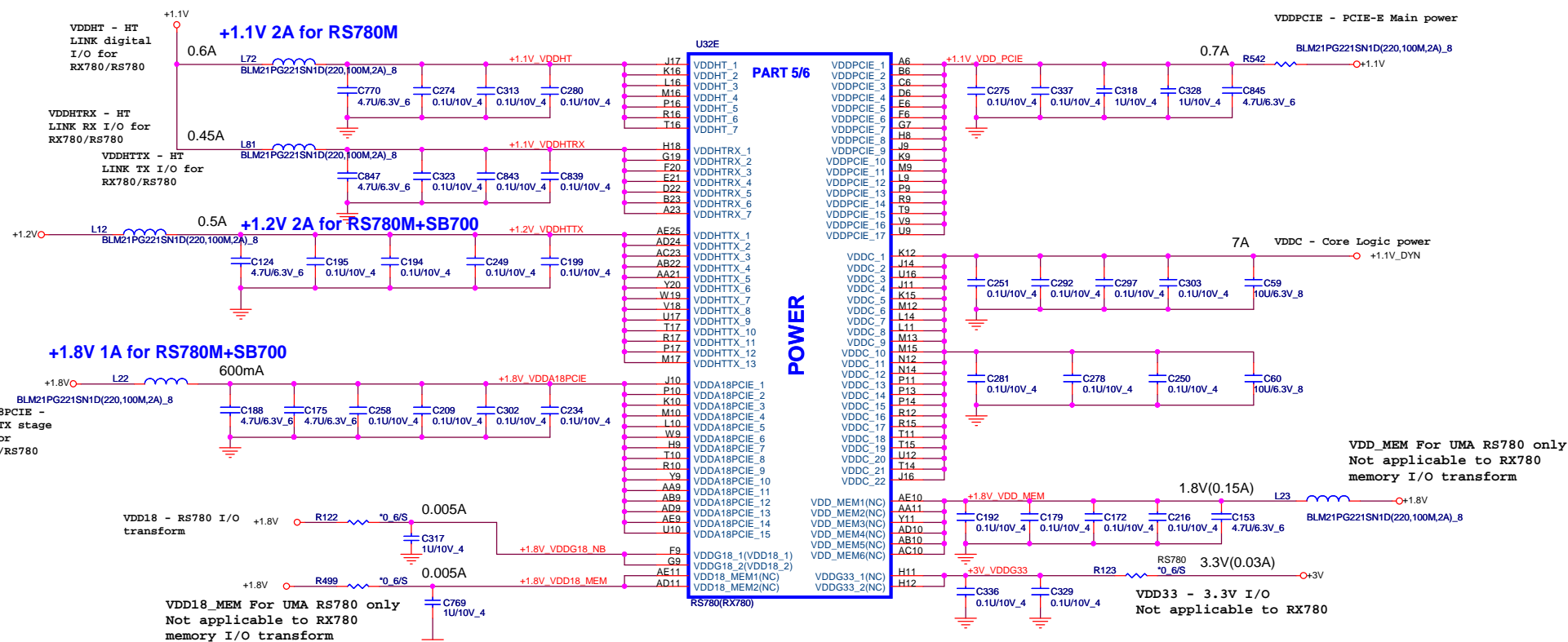








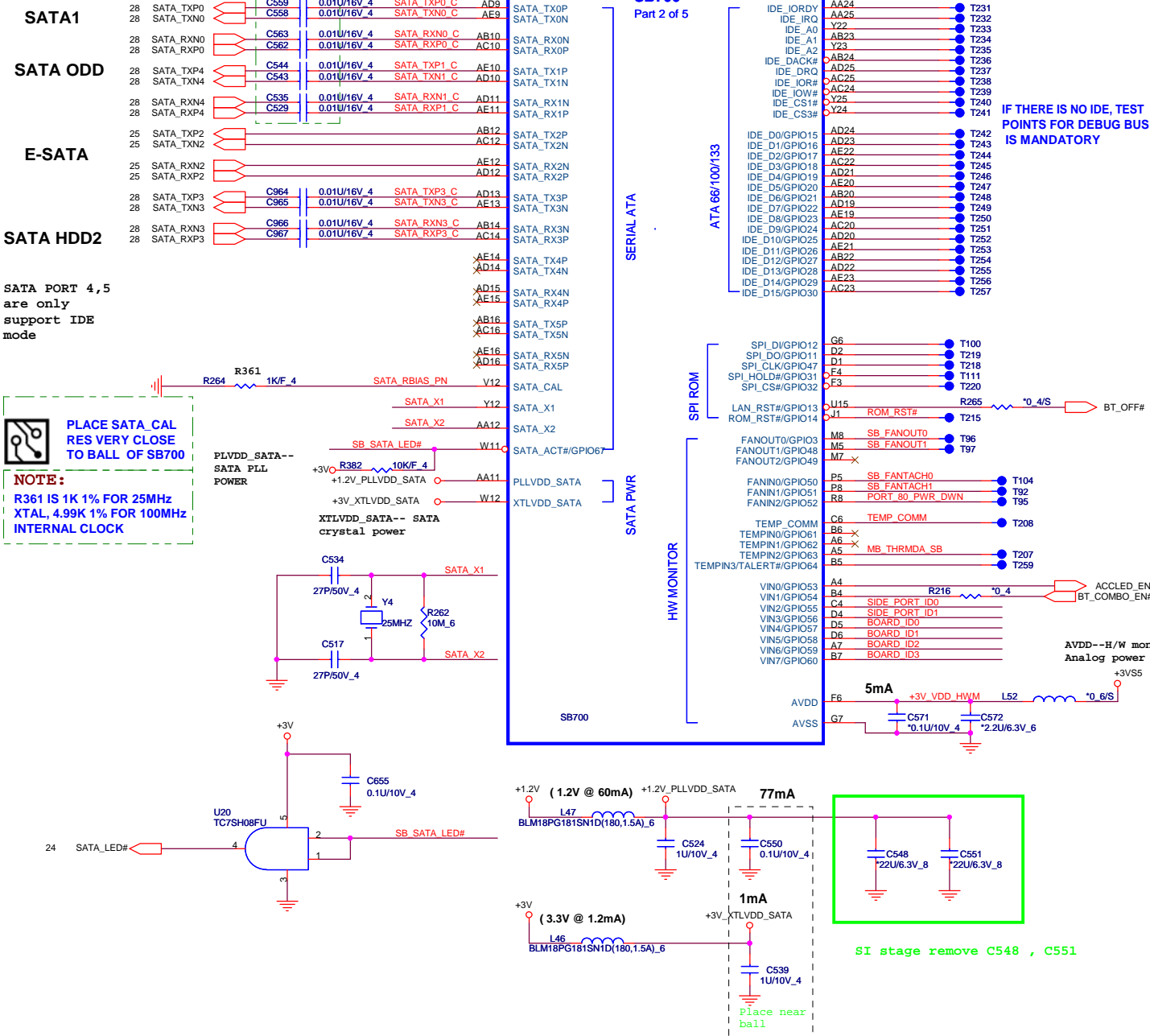
PIN NAME	RX780	RS780	PIN NAME	RX780	RS780
VDDHT	+1.1V	+1.1V	IOPLLVDD	NC	+1.1V
VDDHTRX	+1.1V	+1.1V	AVDD	NC	+3.3V
VDDHTTX	+1.2V	+1.2V	AVDDDI	NC	+1.8V
VDDA18PCIE	+1.8V	+1.8V	AVDDQ	NC	+1.8V
VDDG18	+1.8V	+1.8V	PLLVD	NC	+1.1V
VDD18_MEM	NC	+1.8V	PLLVD18	NC	+1.8V
VDDPCIE	+1.1V	+1.1V	VDDA18PCIEPLL	+1.8V	+1.8V
VDDC	+1.1V	+1.1V	VDDA18HTPLL	+1.8V	+1.8V
VDD_MEM	NC	+1.8V/1.5V	VDDLTP18	NC	+1.8V
VDDG33	NC	+3.3V	VDDL18	NC	+1.8V
IOPLLVDD18	NC	+1.8V	VDDL18T33	NC	NC



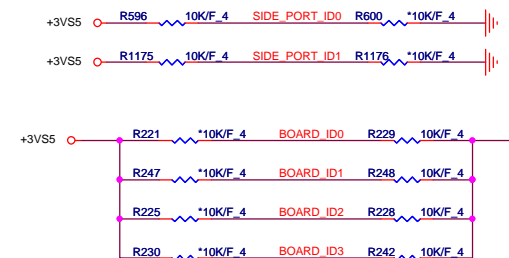




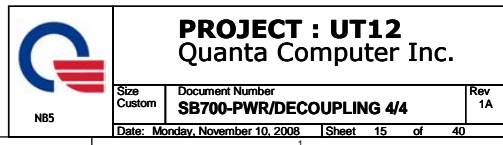




SIDE_PORT_ID1	SIDE_PORT_ID0	
0	0	Samsung
0	1	Qimonda
1	0	Hynix
1	1	no support side port



ID3	ID2	ID1	ID0	
0	0	0	0	UT1 UMA
0	0	0	1	UT2 UMA
0	0	1	0	UT1 M92
0	0	1	1	UT2 M92
0	1	0	0	UT1 M96
0	1	0	1	UT2 M96
0	1	1	0	
0	1	1	1	

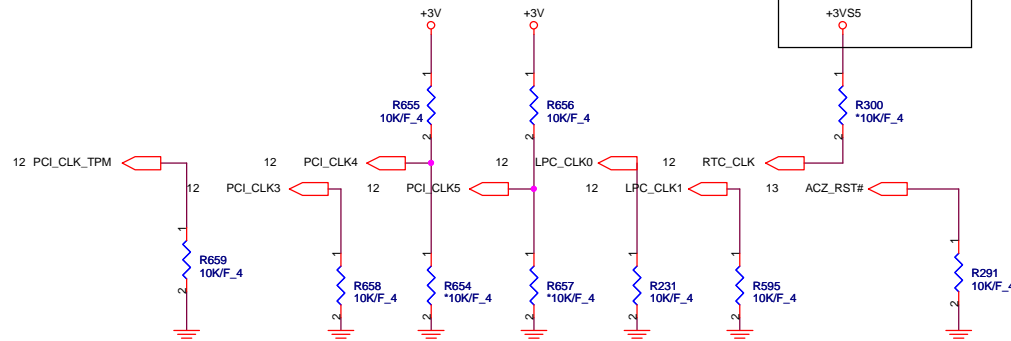




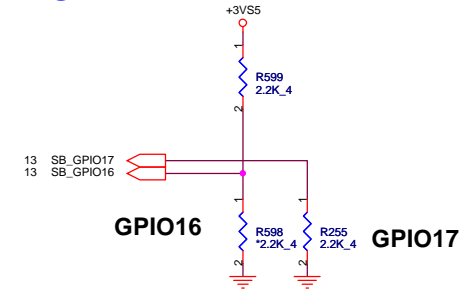
OVERLAP COMMON PADS WHERE POSSIBLE FOR DUAL-OF RESISTORS.

It must ready  
before RSMRST#

## REQUIRED STRAPS



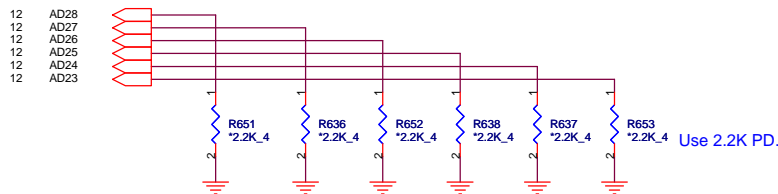
	PCI_CLK_TPM	PCI_CLK3	PCI_CLK4	PCI_CLK5	LPC_CLK0	LPC_CLK1	RTC_CLK	AZ_RST#
PULL HIGH	BOOTFAIL TIMER ENABLED	USE DEBUG STRAPS	RESERVED	RESERVED	IMC ENABLED	CLKGEN ENABLED	INTERNAL RTC  DEFAULT	ENABLE PCI ROM BOOT
PULL LOW	BOOTFAIL TIMER DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT			IMC DISABLED DEFAULT	CLKGEN DISABLED DEFAULT	EXT. RTC (PD on X1, apply 32KHz to RTC_CLK)	DISABLE PCI ROM BOOT DEFAULT



TYPE	GPIO16	GPIO17
FWH	L : 2.2K pull down	L : 2.2K pull down
LPC	NC	L : 2.2K pull down
SPI	L : 2.2K pull down	NC
RSVD	NC	NC

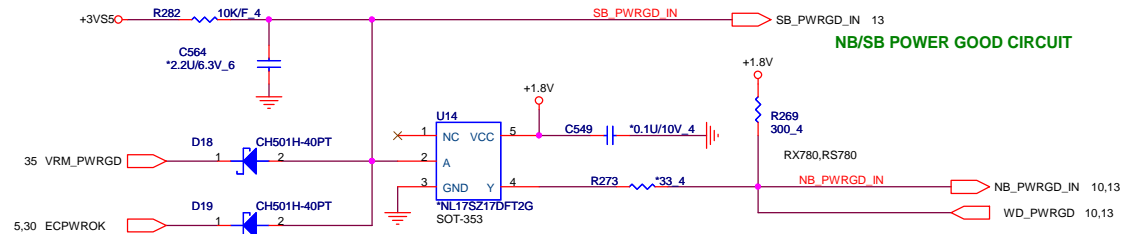
## DEBUG STRAPS

SB700 HAS 15K INTERNAL PU FOR PCI\_AD[28:23]



	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE LONG RESET DEFAULT	USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	RESERVED
PULL LOW	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	

NB\_PWRGD\_IN:  
RS780/RX780 = 1.8V; RS740 = 3.3V  
Do NOT share it with SB\_PWRGD when use Internal Clk Gen  
(Need SB PLL initialize firstly)



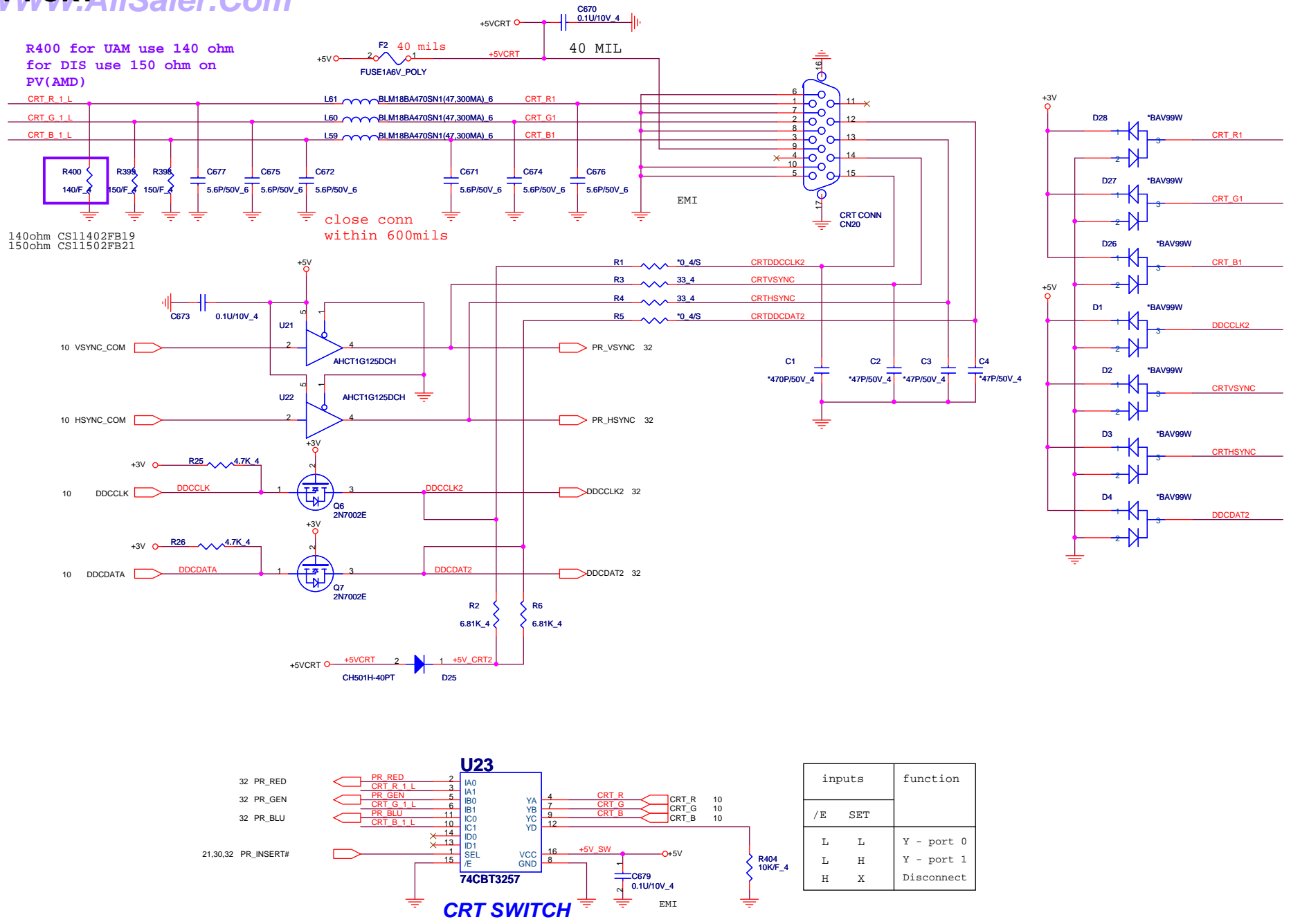
AL17SZ17000 IC(5P) NL17SZ17DFT2G(SOT-353) SOT-353  
ALUC1G17000 IC OTHER(5P) SN74AUC1G17DBVR(SOT23-5) SOT23-5

**PROJECT : UT12**  
Quanta Computer Inc.

Size Custom	Document Number <b>SB700-STRAPS</b>	Rev 1A
Date: Monday, November 10, 2008   Sheet 16 of 40		

CRT PORT

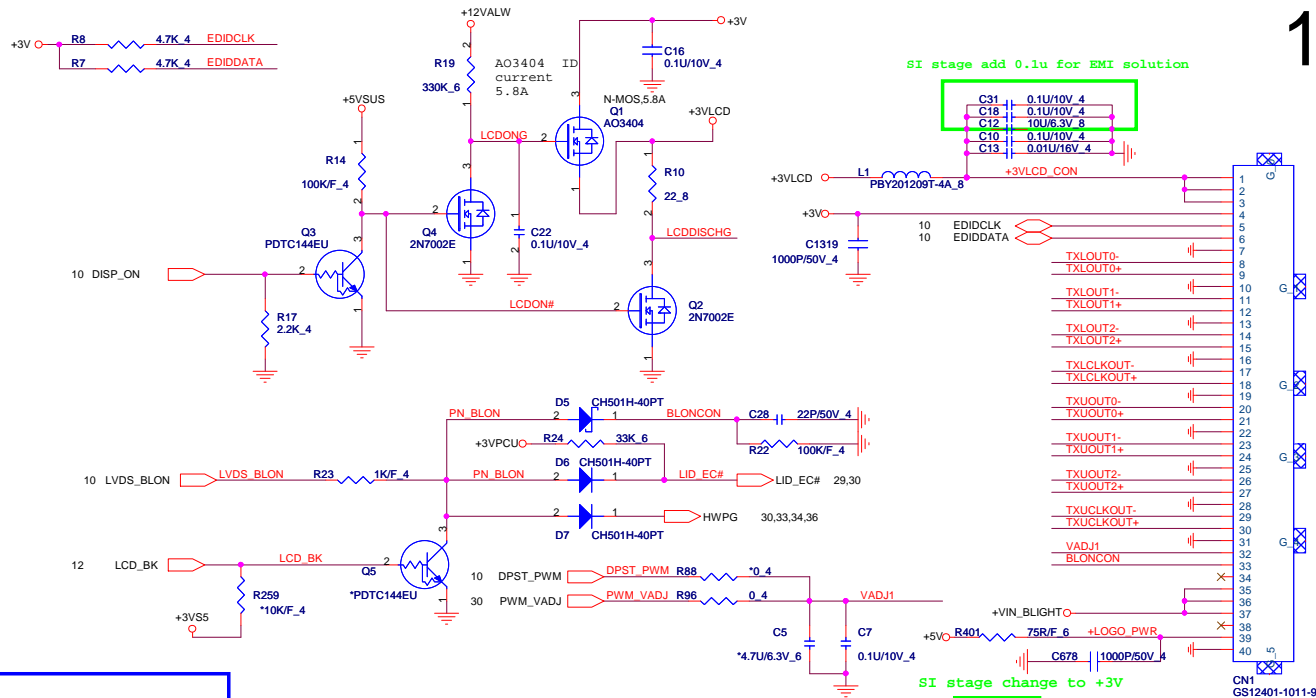
R400 for UAM use 140 ohm  
for DIS use 150 ohm on  
PV(AMD)



inputs		function
/E	SET	
L	L	Y - port 0
L	H	Y - port 1
H	X	Disconnect

OPTION SIGNAL FROM NB to LVDS for UMA

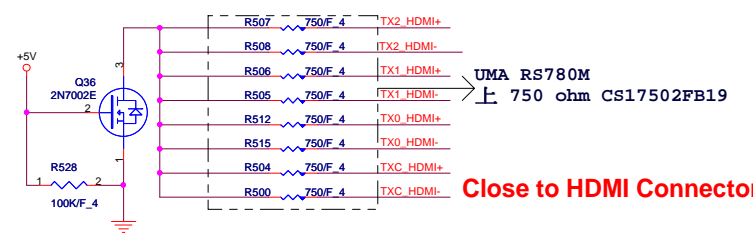
10	LA_CLK	LA_CLK	TXCLKOUT+
10	LA_CLK#	LA_CLK#	TXCLKOUT-
10	LA_DATAP0	LA_DATAP0	TXOUT0+
10	LA_DATAN0	LA_DATAN0	TXOUT0-
10	LA_DATAP1	LA_DATAP1	TXOUT1+
10	LA_DATAN1	LA_DATAN1	TXOUT1-
10	LA_DATAP2	LA_DATAP2	TXOUT2+
10	LA_DATAN2	LA_DATAN2	TXOUT2-
10	LB_CLK	LB_CLK	TXCLKOUT+
10	LB_CLK#	LB_CLK#	TXCLKOUT-
10	LB_DATAP0	LB_DATAP0	TXUOUT0+
10	LB_DATAN0	LB_DATAN0	TXUOUT0-
10	LB_DATAP1	LB_DATAP1	TXUOUT1+
10	LB_DATAN1	LB_DATAN1	TXUOUT1-
10	LB_DATAP2	LB_DATAP2	TXUOUT2+
10	LB_DATAN2	LB_DATAN2	TXUOUT2-



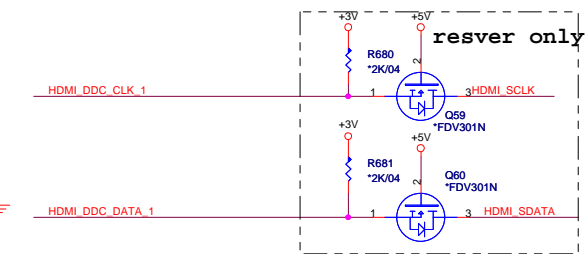
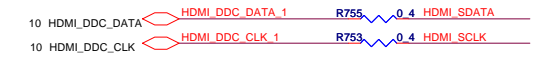
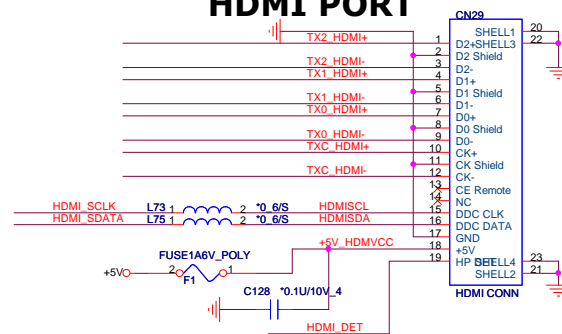
From RS780M

For Layout concern, placement close north bridge

9	C_PEG_TX#15	C_PEG_TX#15	C386	0.1u/10V_4	TX2 HDMI-L	TX2 HDMI-
9	C_PEG_TX#15	C_PEG_TX#15	C387	0.1u/10V_4	TX2 HDMI+L	TX2 HDMI+
9	C_PEG_TX#14	C_PEG_TX#14	C388	0.1u/10V_4	TX1 HDMI-L	TX1 HDMI-
9	C_PEG_TX#14	C_PEG_TX#14	C389	0.1u/10V_4	TX1 HDMI+L	TX1 HDMI+
9	C_PEG_TX#13	C_PEG_TX#13	C355	0.1u/10V_4	TX0 HDMI-L	TX0 HDMI-
9	C_PEG_TX#13	C_PEG_TX#13	C344	0.1u/10V_4	TX0 HDMI+L	TX0 HDMI+
9	C_PEG_TX#12	C_PEG_TX#12	C827	0.1u/10V_4	TXC HDMI-L	TXC HDMI-
9	C_PEG_TX#12	C_PEG_TX#12	C828	0.1u/10V_4	TXC HDMI+L	TXC HDMI+



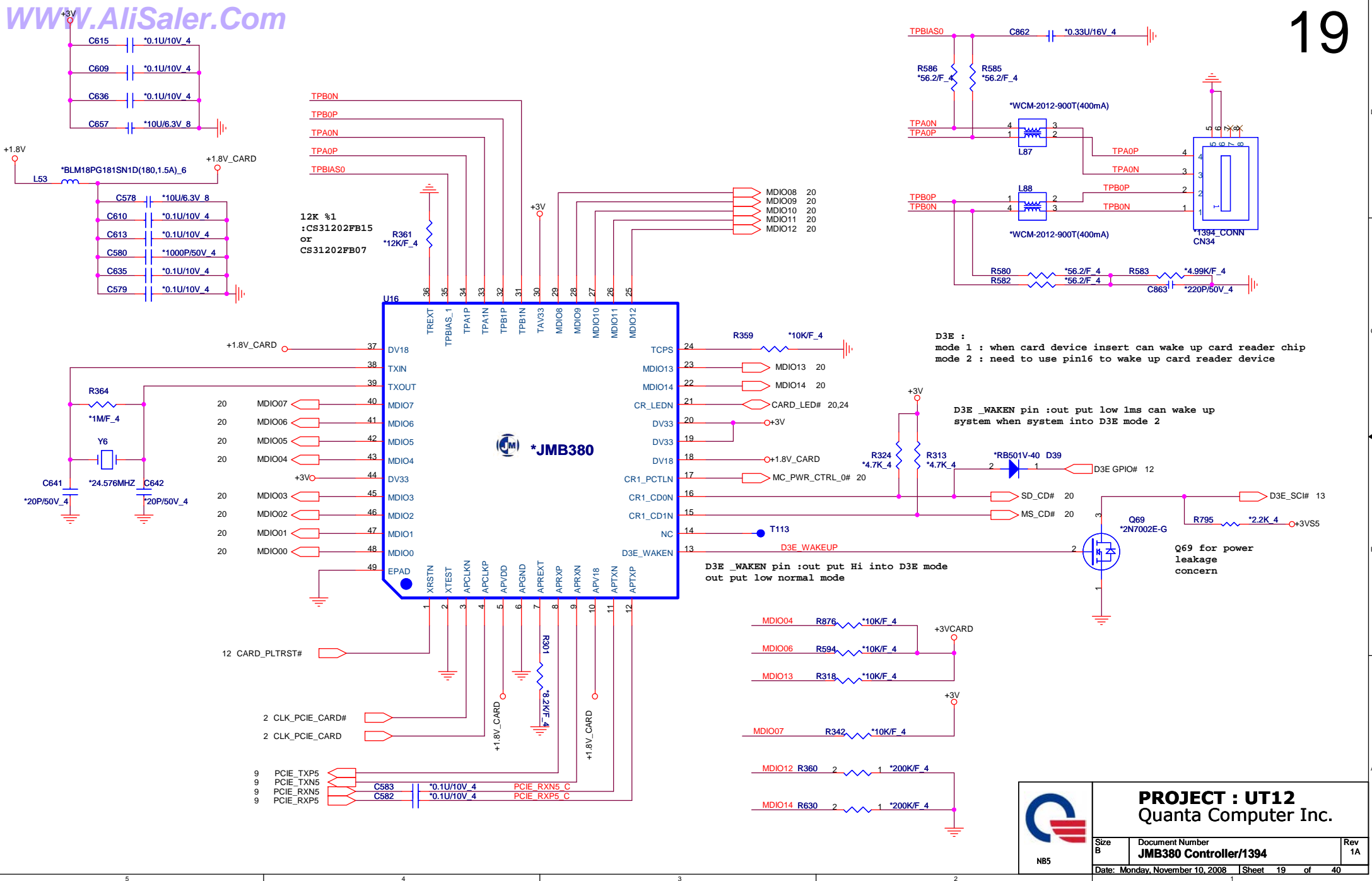
HDMI PORT



**PROJECT : UT12**  
Quanta Computer Inc.

Size Custom	Document Number <b>LCD CONN,HDMI CONN</b>	Rev 1A
Date: Monday, November 10, 2008		Sheet 18 of 40



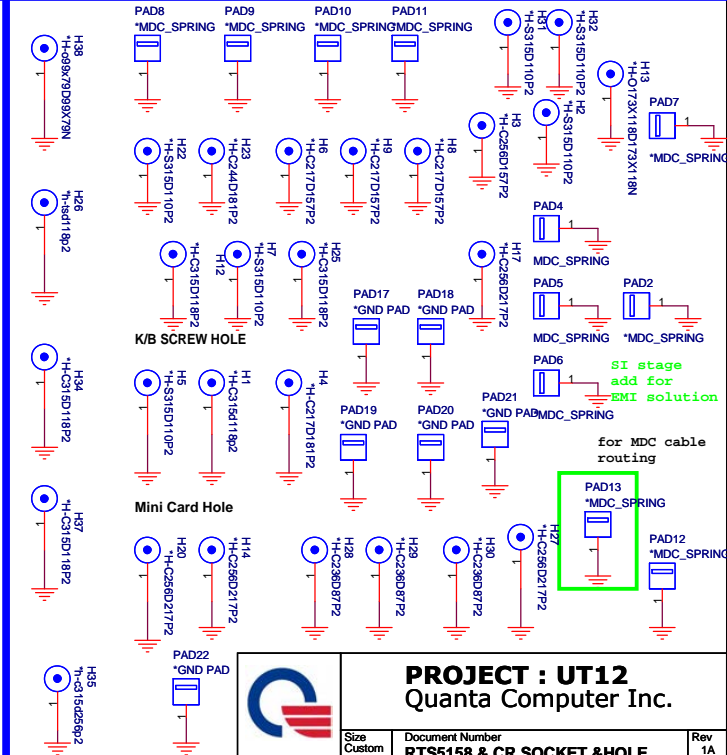
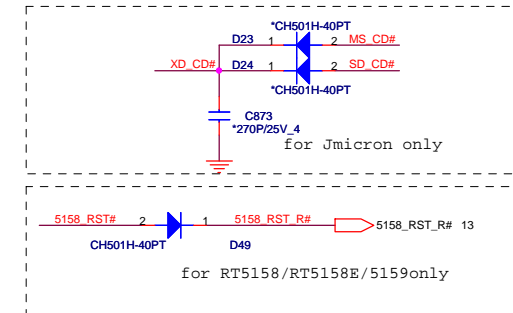


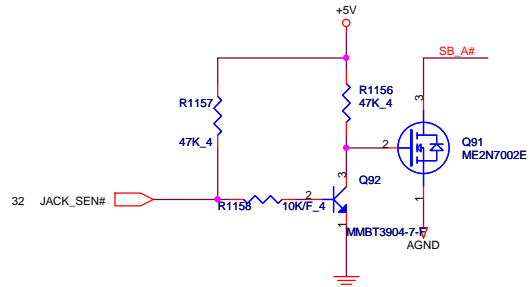
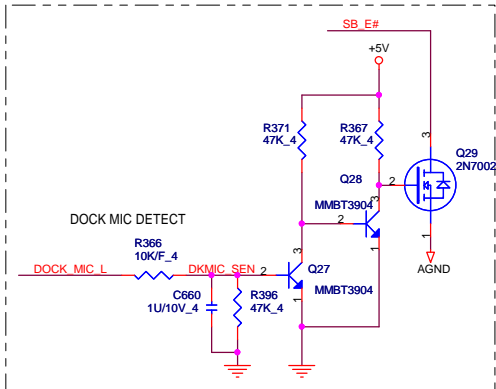
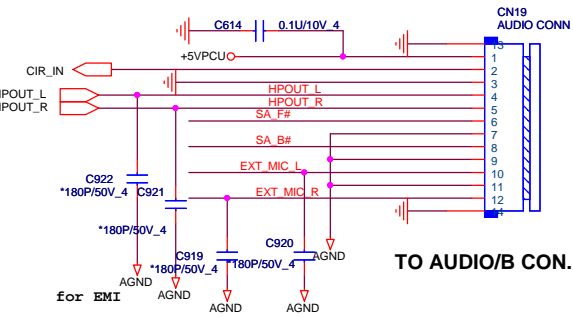
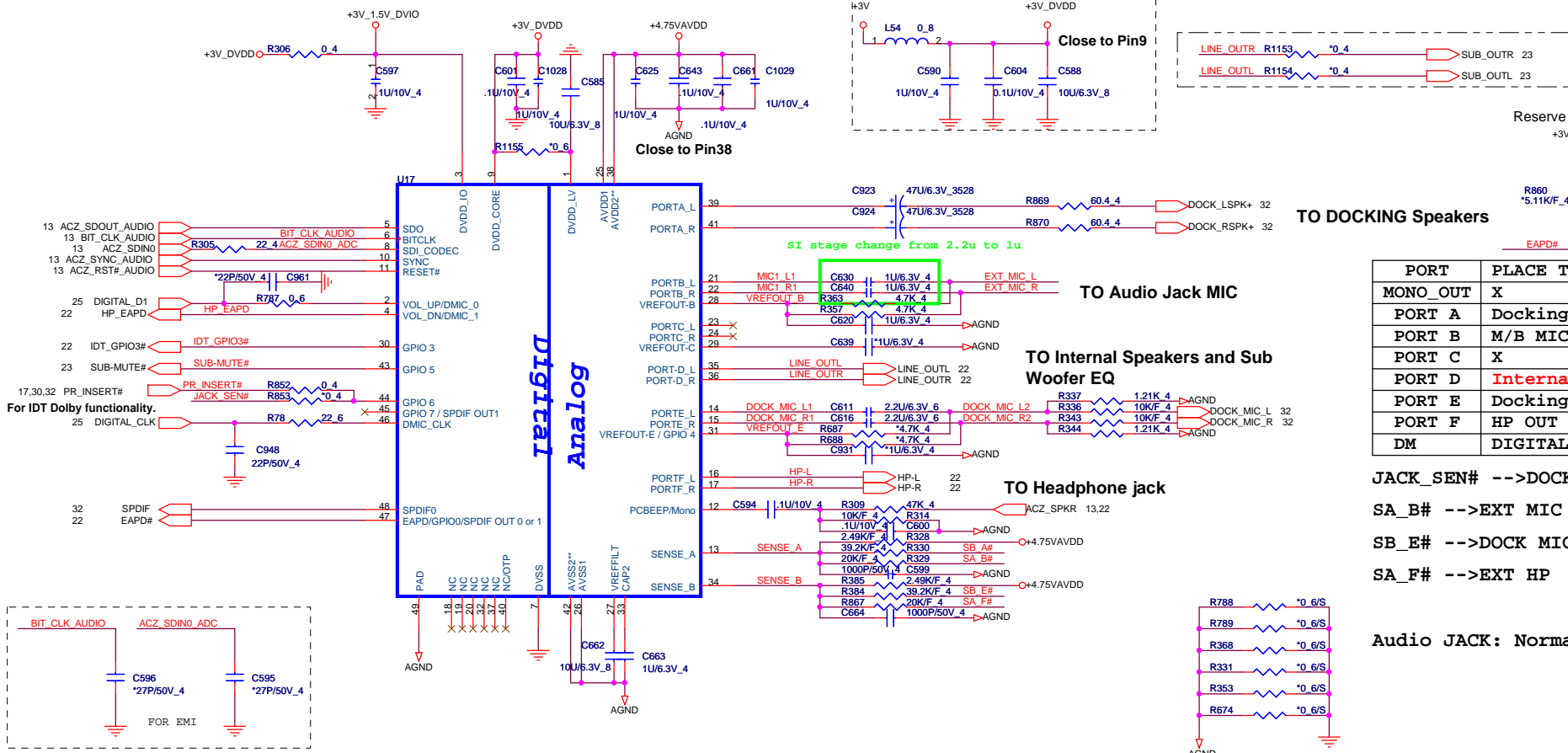
**PROJECT : UT12**  
Quanta Computer Inc.

Size B	Document Number <b>JMB380 Controller/1394</b>	Rev 1A
Date: Monday, November 10, 2008	Sheet 19	of 40



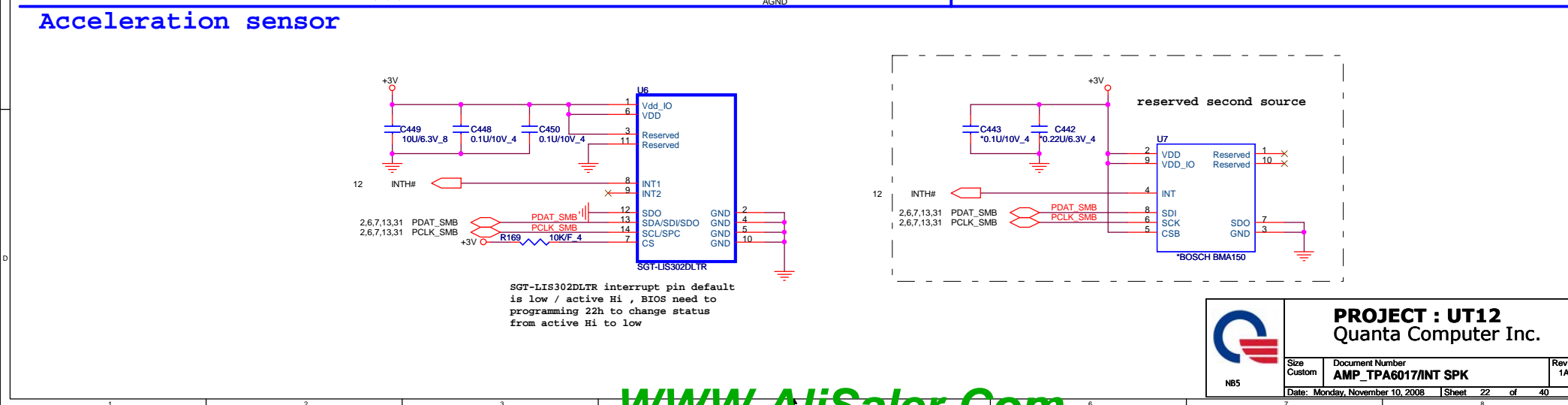
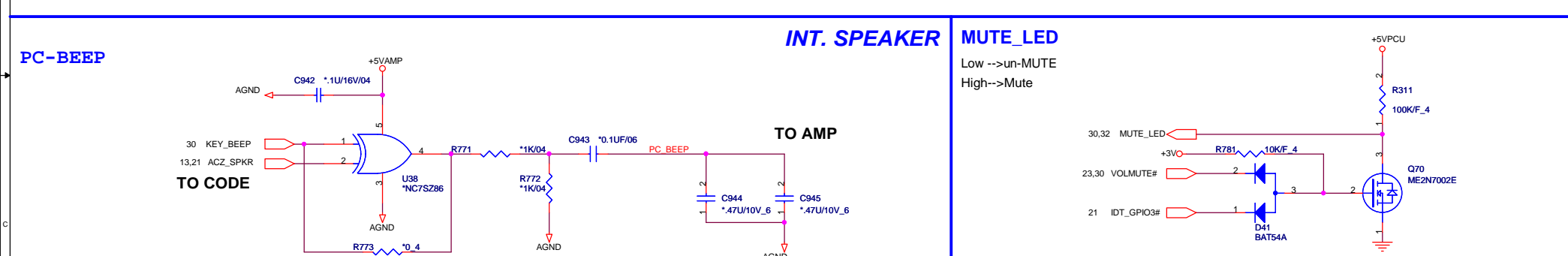
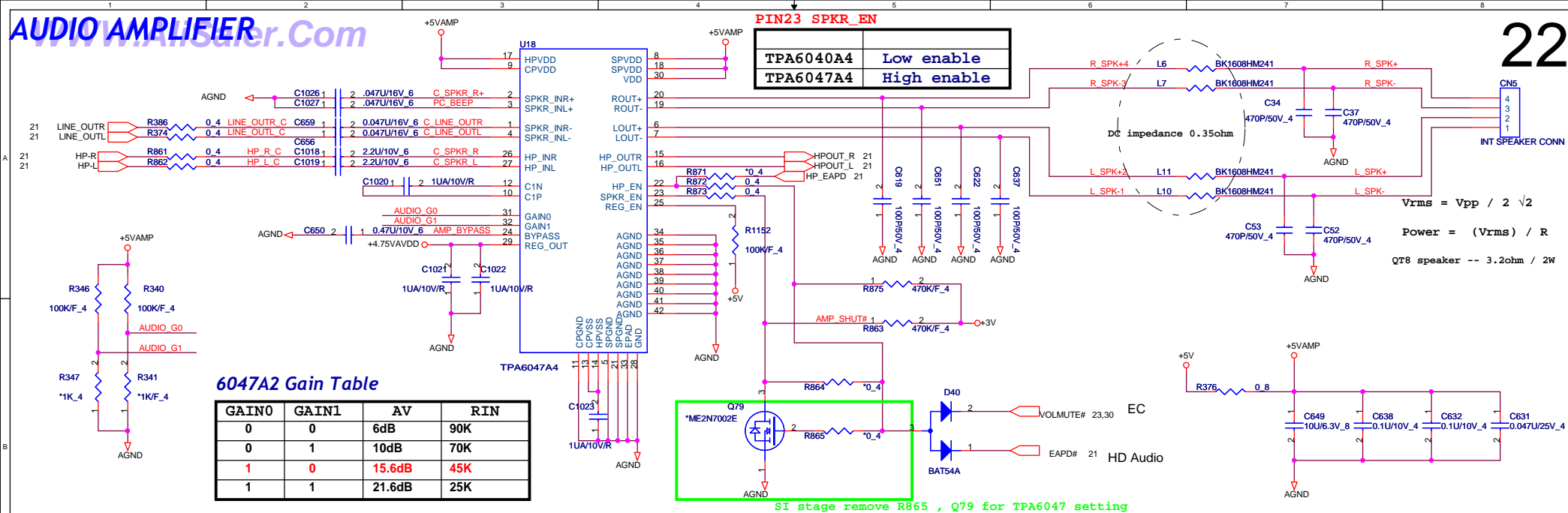
SP7	R315	0.4	MS_DATA0	SD_DATA0
	R316	0.4		XD-D6
SP6	R334	0.4		MS_DATA1
	R335	0.4		XD-D3
SP8	R345	0.4	MS_DATA2	XD-D2
SP16	R666	0.4	SD_DATA2	XD-D2
	R676	0.4		XD-RE#
SP5	R327	0.4		MS_B5
	R328	0.4		XD-D5
SP15	R675	0.4	SD_DATA3	XD-D3
	R390	0.4		XD_WE
SP11	R354	0.4	SD_CLK	MS_CLK
	R368	0.4		XD-D1
SP2	R317	0.4		SD_WP
SP13	R677	0.4		XD-WP#
SP19	R393	0.4		XD-CLE
SP4	R317	0.4		XD-D4
SP10	R365	0.4	MS_DATA3	
	R348	0.4		XD-D7
SP14	R389	0.4		XD-RB#
SP12	R369	0.4		XD-D0
SP17	R391	0.4		XD-ALE
SP3	R398	0.4		XD-CE#
SD_CMD_R	R372	0.4		SD_CMD
SP4	R333	0.4		SD_DATA1

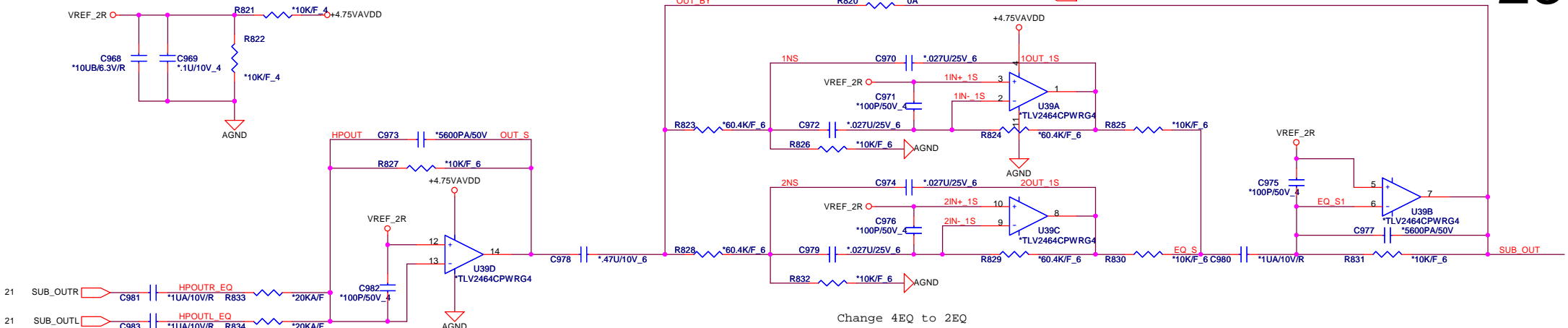




**PROJECT : UT12**  
**Quanta Computer Inc.**

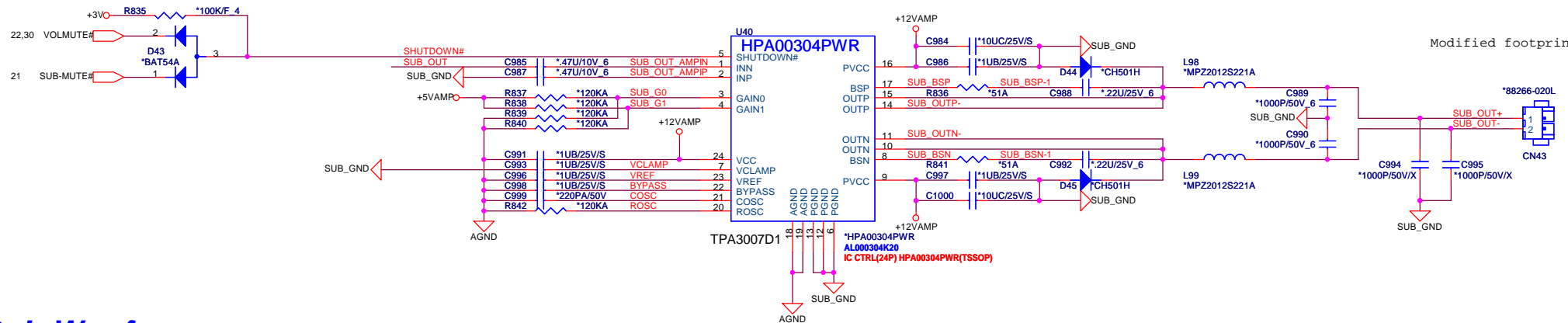
Size Custom Document Number  
**Azalia AD1883**  
 Date: Monday, November 10, 2008 Sheet 21 of 40  
 Rev 1A



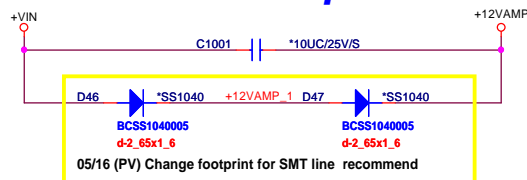


MODEL	UT1	UT2
R823	60.4K/F_6	40.2K/F_6
R824	60.4K/F_6	40.2K/F_6
R828	60.4K/F_6	80.6K/F_6
R829	60.4K/F_6	80.6K/F_6
C970	0.027U/25V_6	0.022U/50V_6
C972	0.027U/25V_6	0.022U/50V_6
C974	0.027U/25V_6	0.039U/16V_6
C976	0.027U/25V_6	0.039U/16V_6

Change 4EQ to 2EQ



## Sub-Woofer power

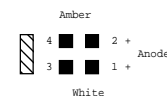


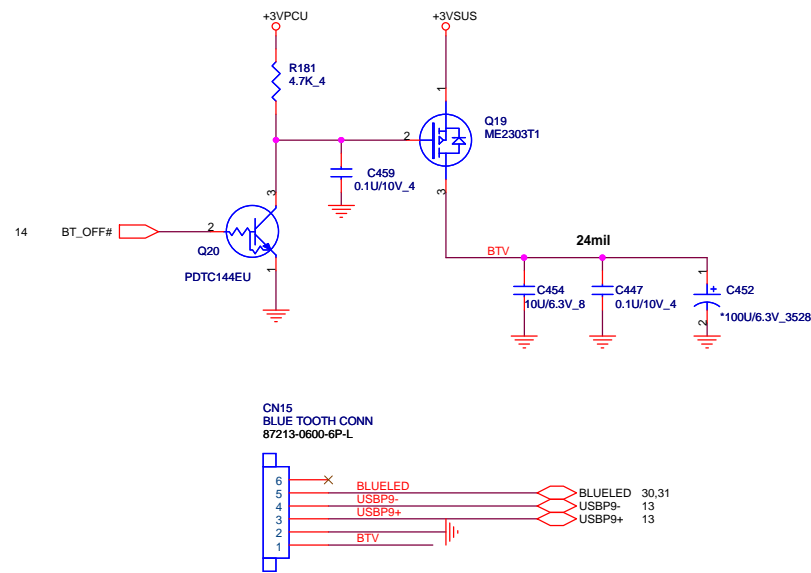
05/16 (PV) Change footprint for SMT line recommend



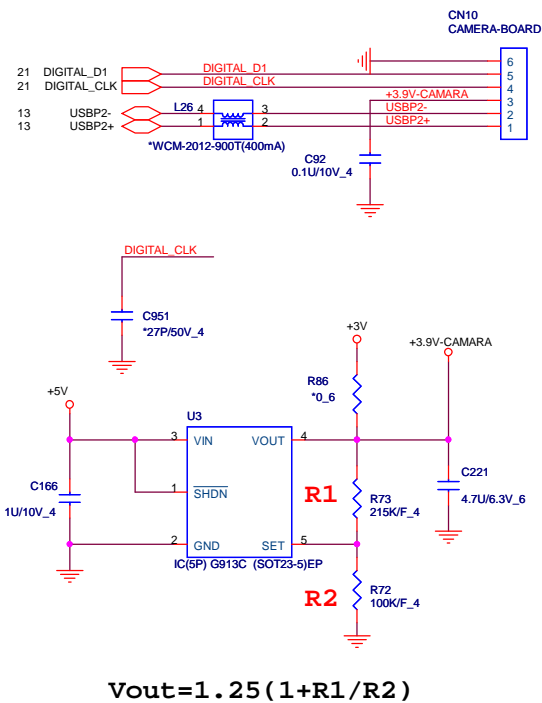


3 White  
Anode 2 1 Amber  
Dual Color ,Right angle  
LTW-326DSKF-5A



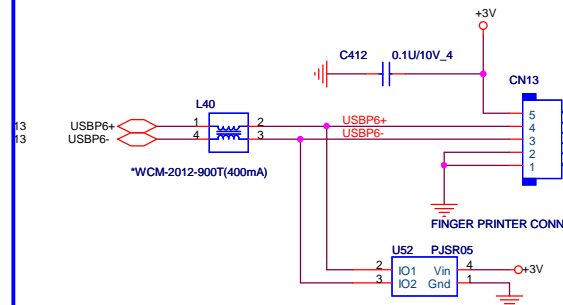


## USB CAMERA CONNECT

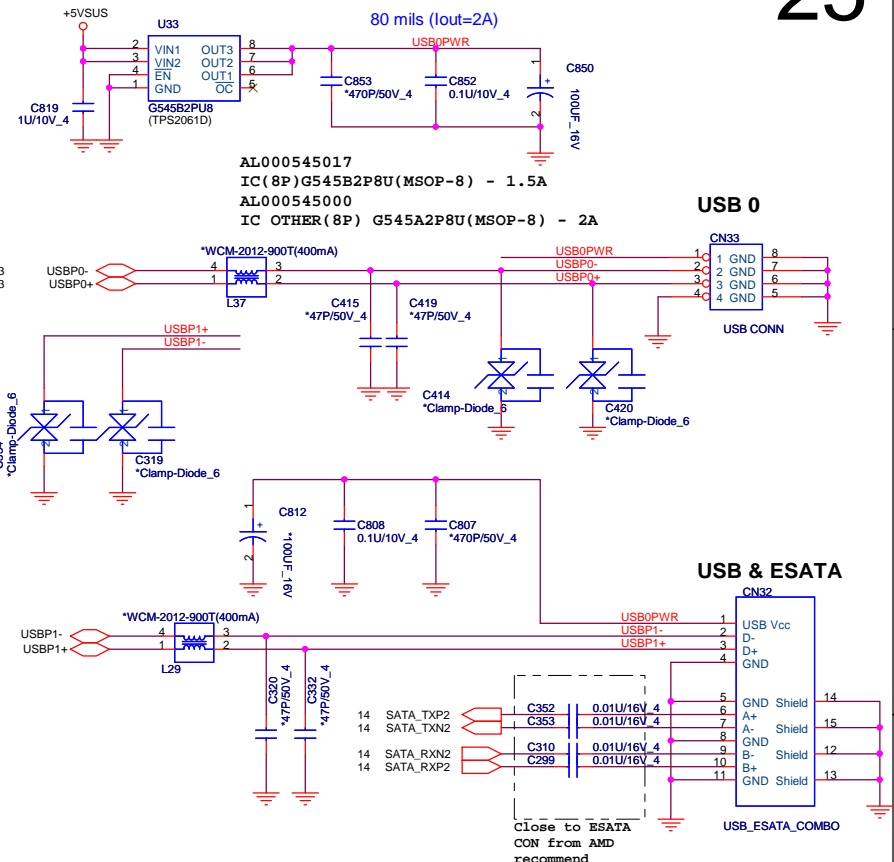


## USB Fingerprint CON

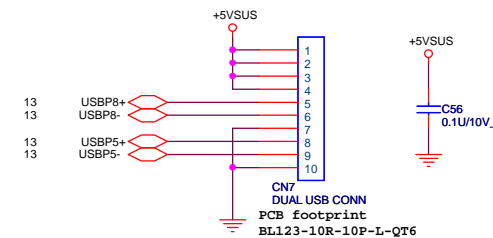
1. ESD GND
2. SYSTEM GND
3. USB-
4. USB+
5. USB PWR(+3V)

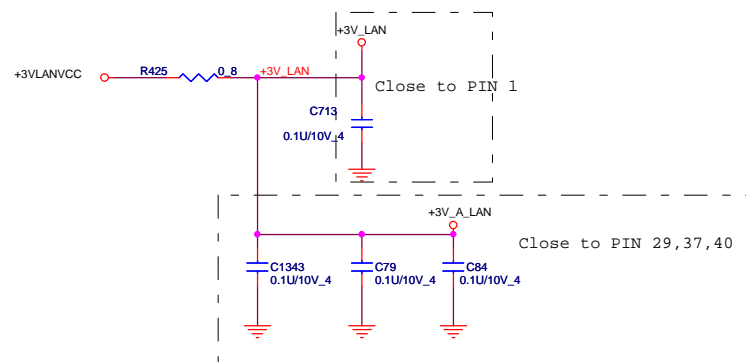


## LEFT SIDE USBX1 and E-SATA/USB COMBO 25

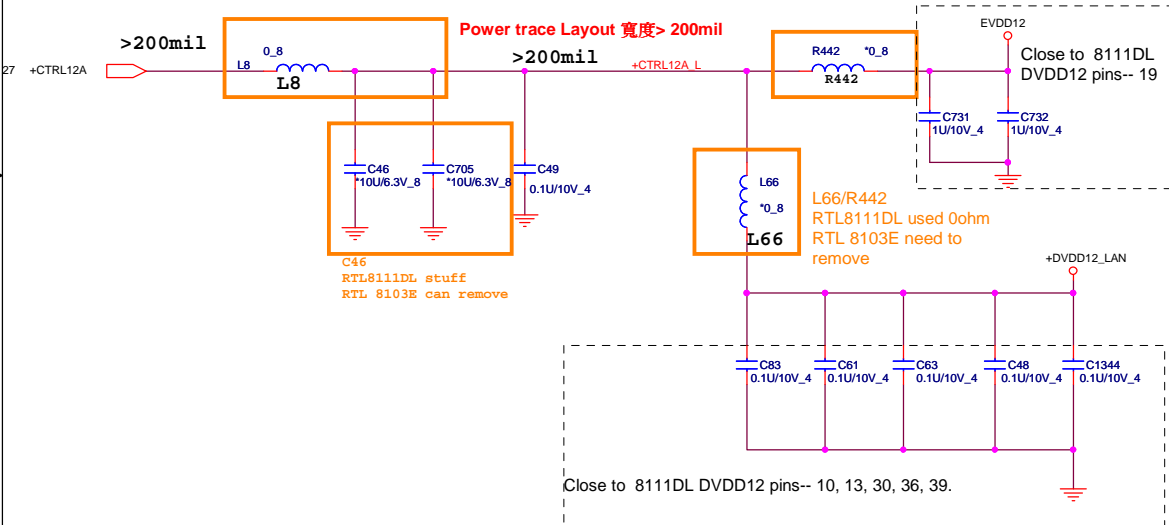


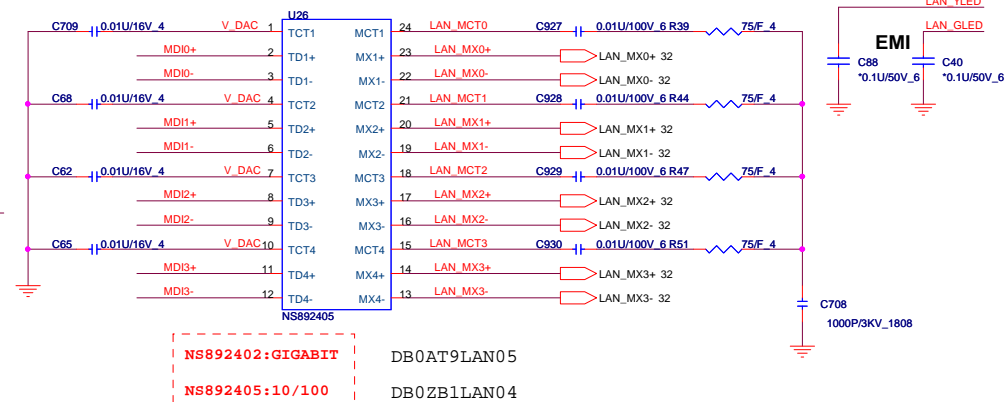
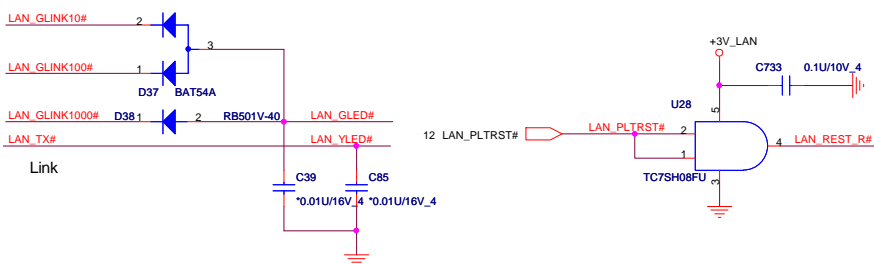
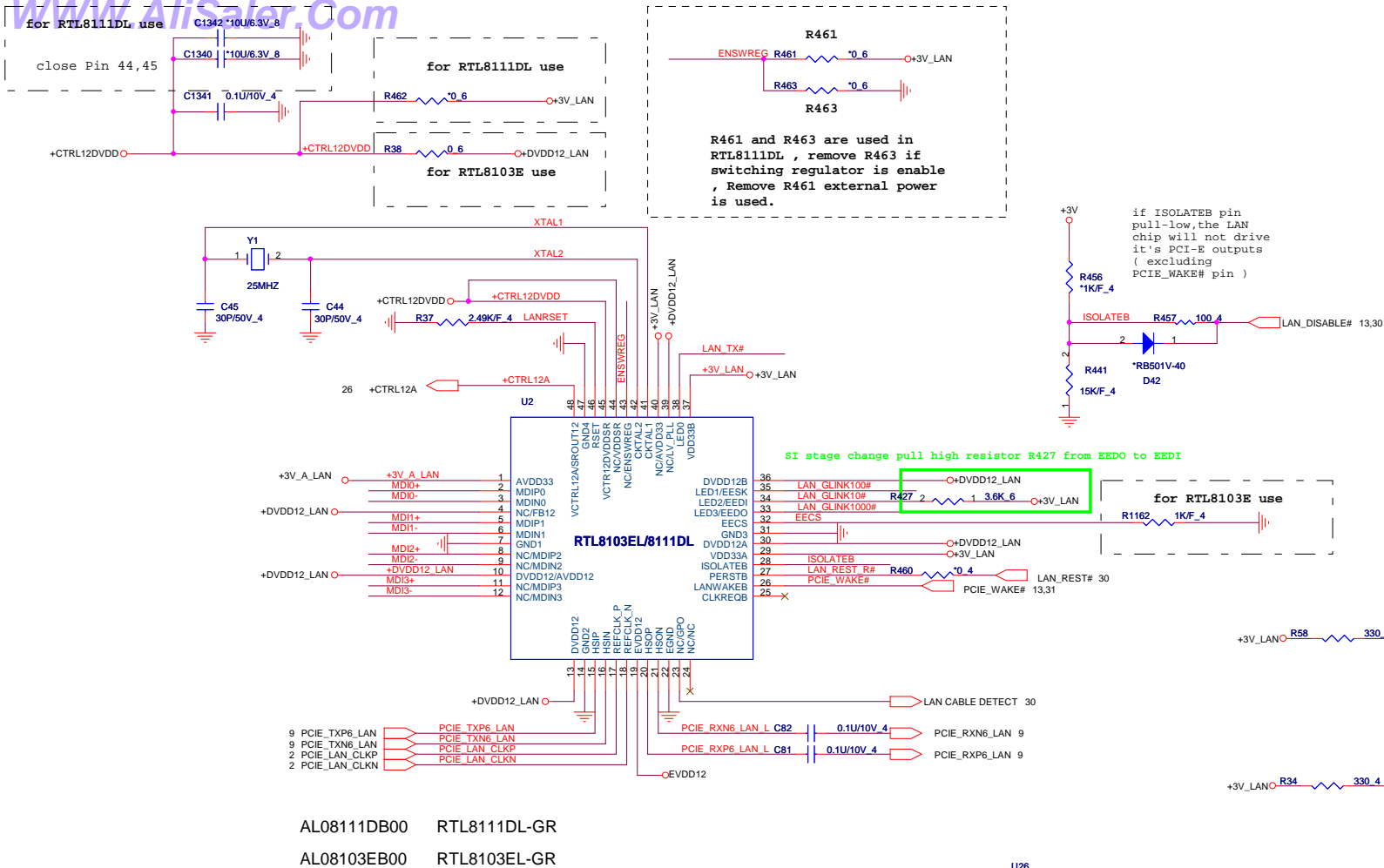
## RIGHT SIDE USBX2

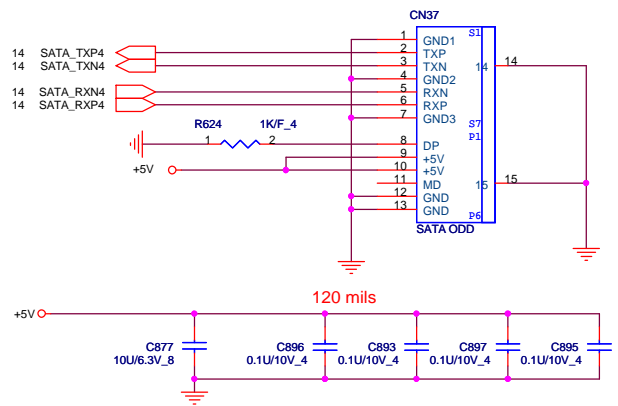




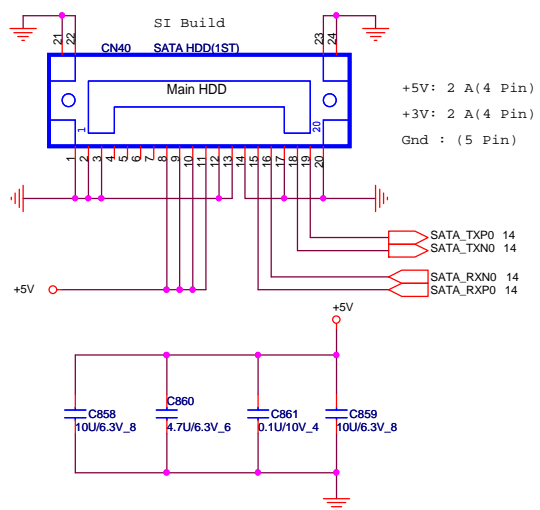
L8  
RTL8111DL (Gaga lan) use 4.7uH  
power choke A>600mA tolerance  
±15%  
RTL8103E stuff 0ohm



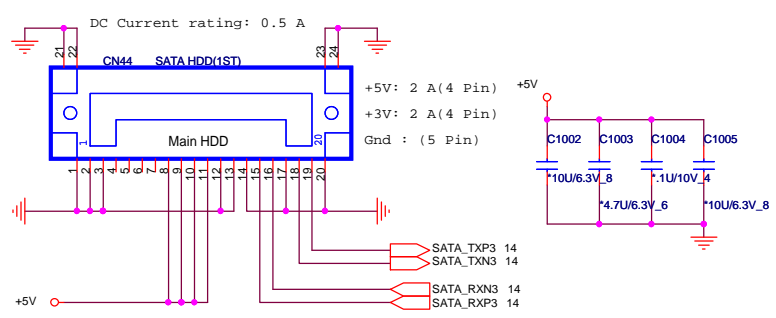




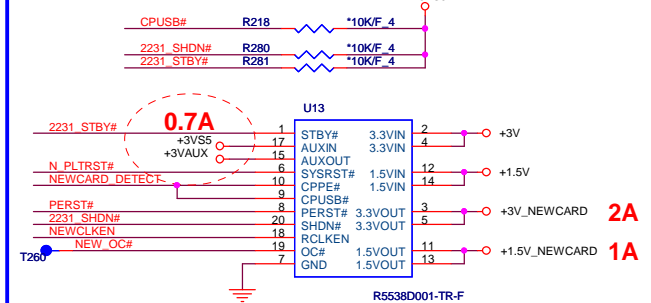
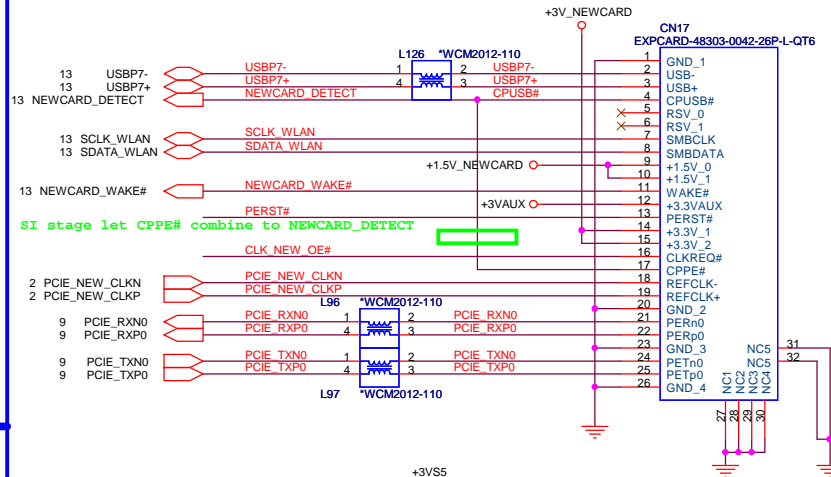
SATA\_1 HDD CONNECTOR



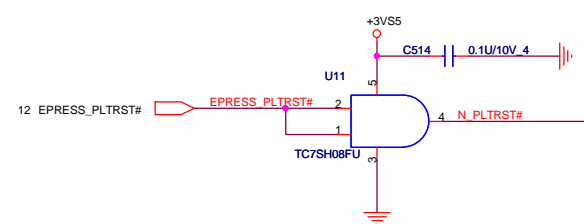
SATA\_2 CONNECTOR



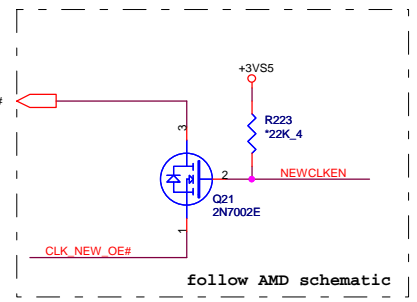
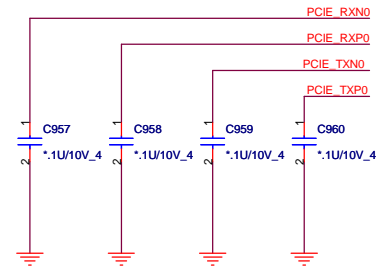
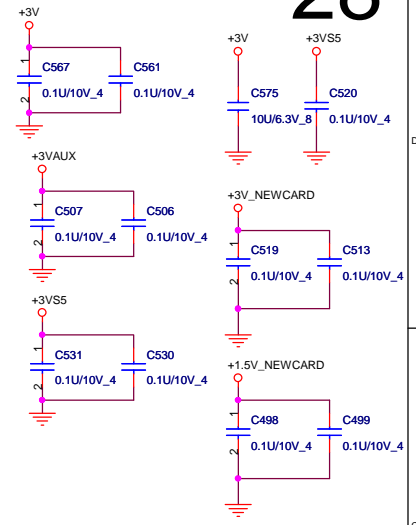
NEWCARD



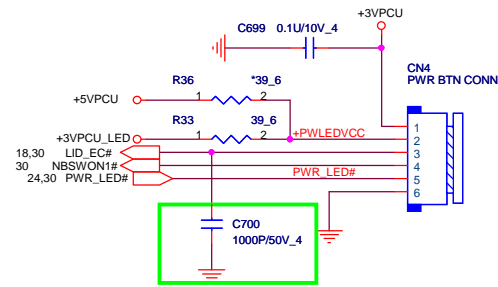
R5538 NEW CARD POWER SWITCH	
pin name	pull hi/low
CPPE#	internal pull up to AUXIN
SYSRST#	internal pull up to AUXIN
CPUSB##	internal pull up to AUXIN
PERST#	a logic level power good
SHDN#	internal pull up to AUXIN
RCLKEN	internal pull up to AUXIN
OC#	over current status
STBY#	internal pull up to AUXIN



NEWCARD (PCIEXPRESS\*1 + USB\*1)

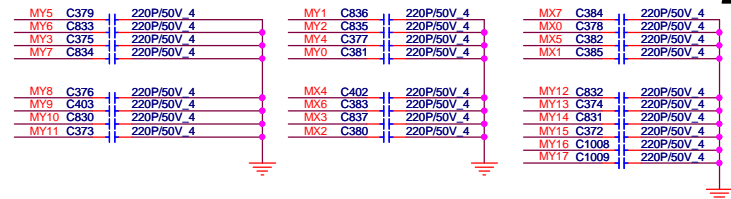




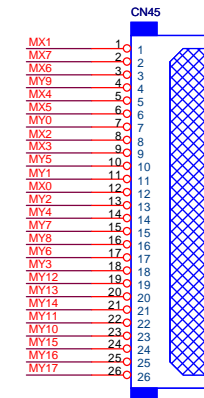
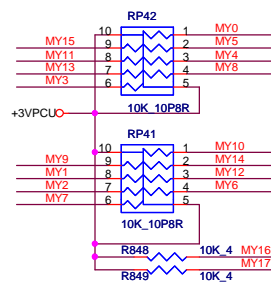


1. +3VPCU(LIDSWITCH PWR)
2. LEDVCC(+3VPCU)
3. LIDSWITCH
4. POWERON#
5. PWRLED#
6. GND

SI stage add 1000P for EMI solution



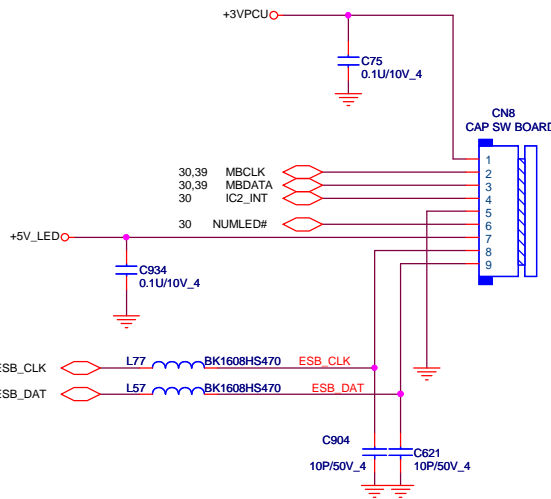
## KEYBOARD PULL-UP



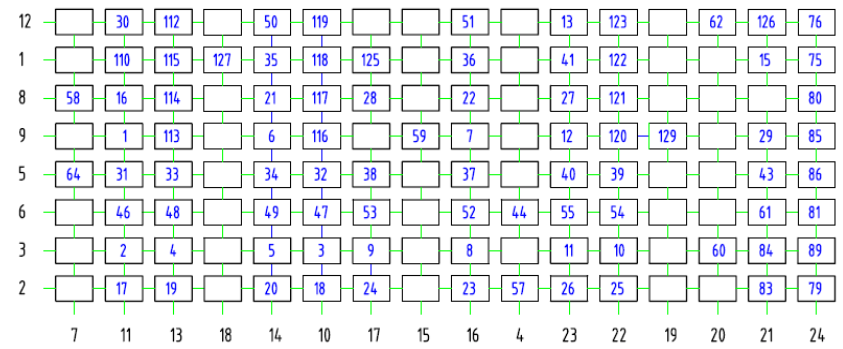
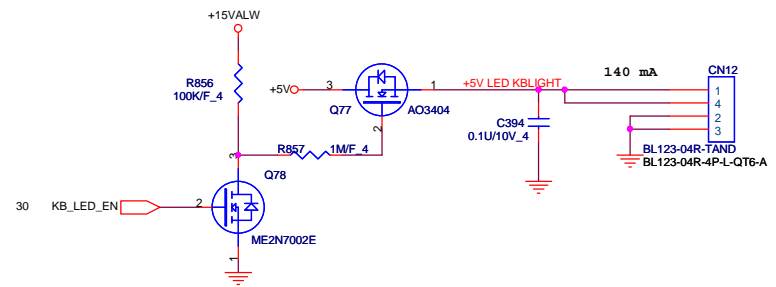
GB1RF260-1253-8

Footprint: "gb1rf260-1253-7f-26p-1

## CAP SW CONNECT

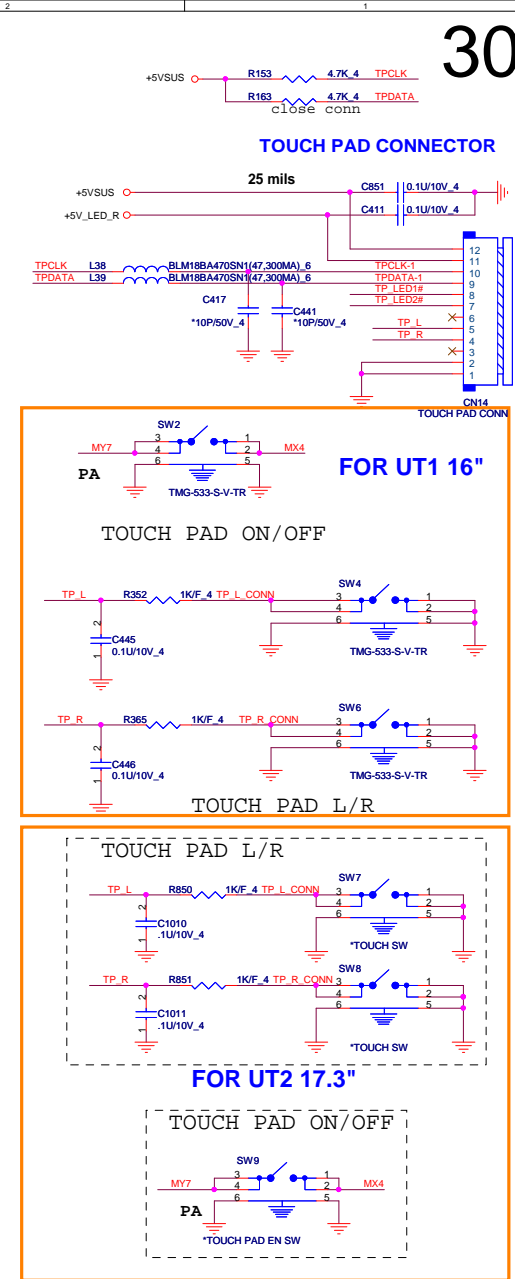


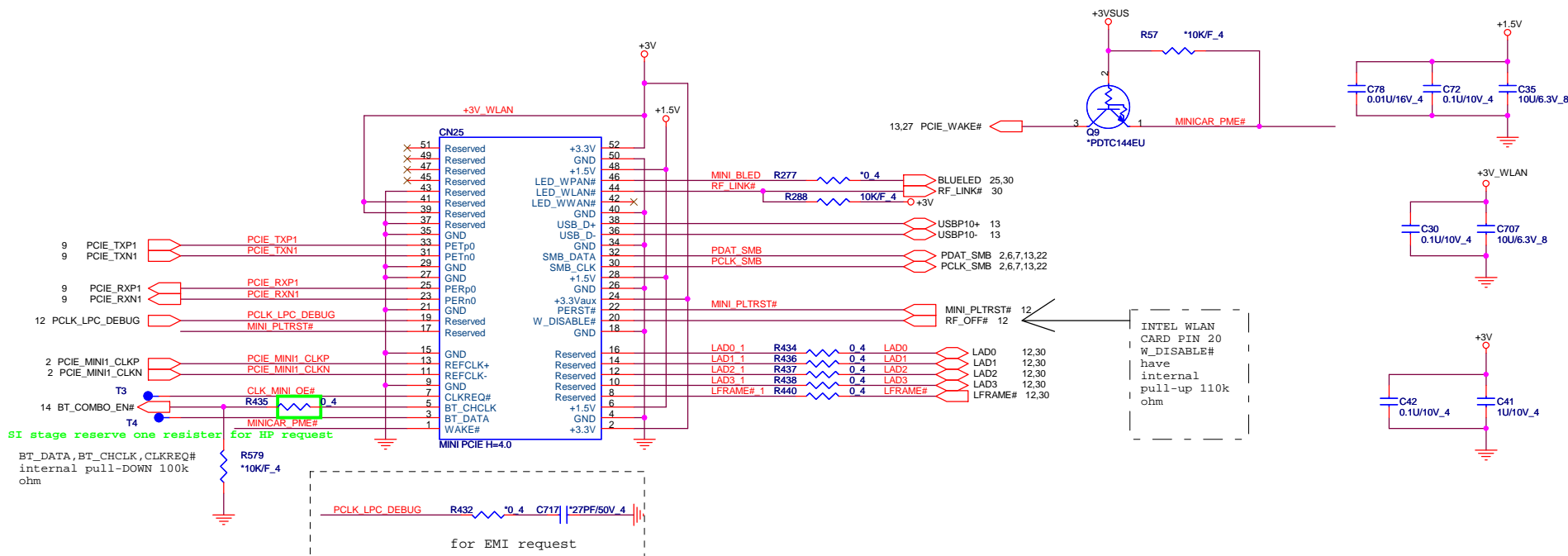
1. +3VPCU
2. MBCLK
3. MBDATA
4. CAP\_INT
5. GND
6. NUM LOCK LED
7. +5V
8. ESB\_CLK
9. ESB\_DAT



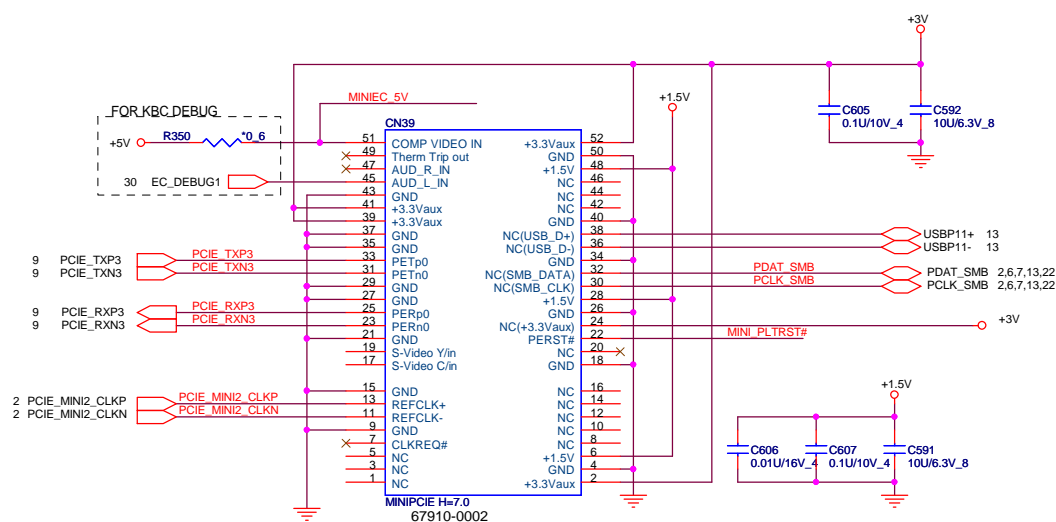
**PROJECT : UT12**  
Quanta Computer Inc.

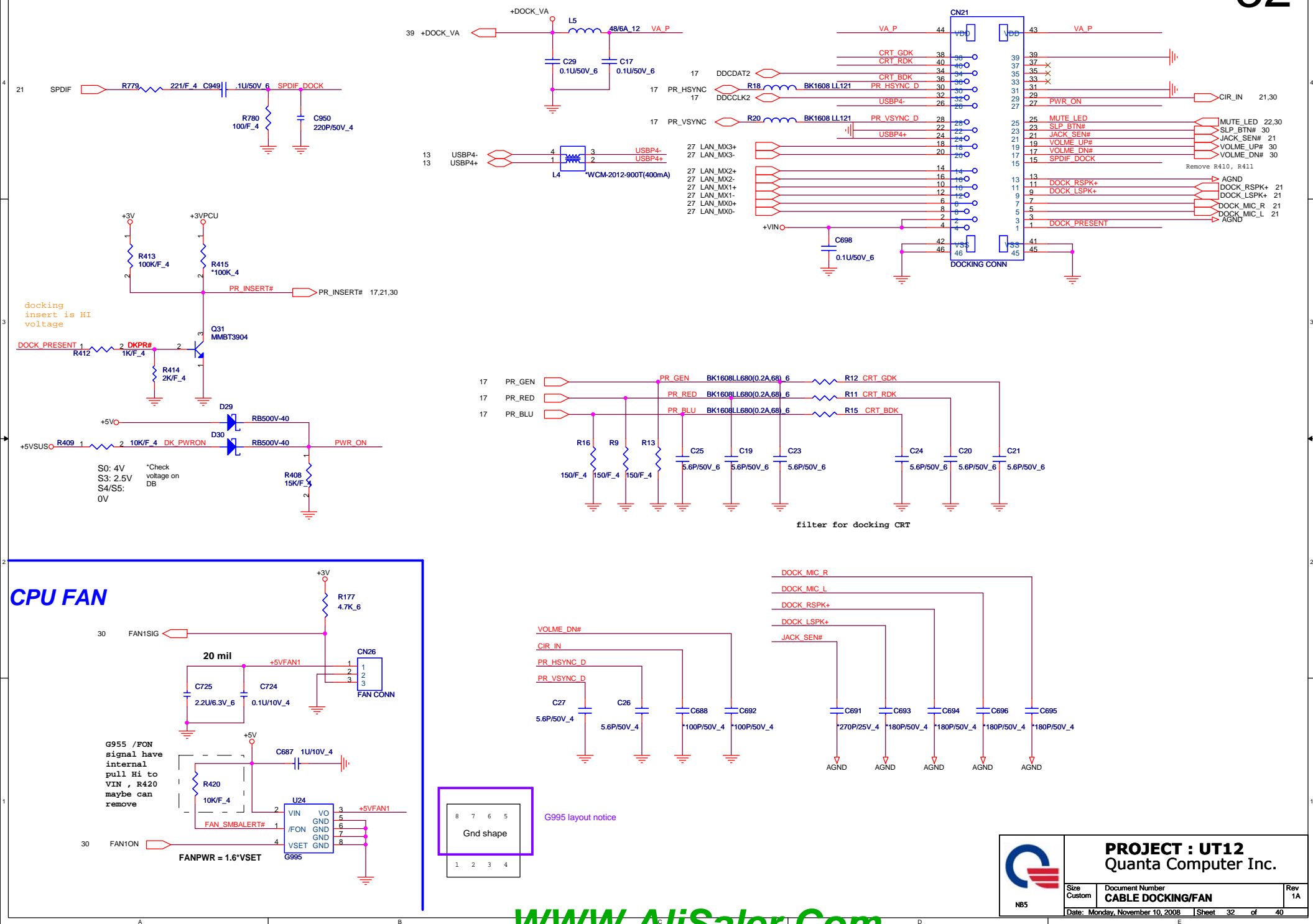
Size Custom	Document Number <b>LED/KEYBOARD/SW</b>	Rev 1A
Date: Monday, November 10, 2008	Sheet 29 of 40	

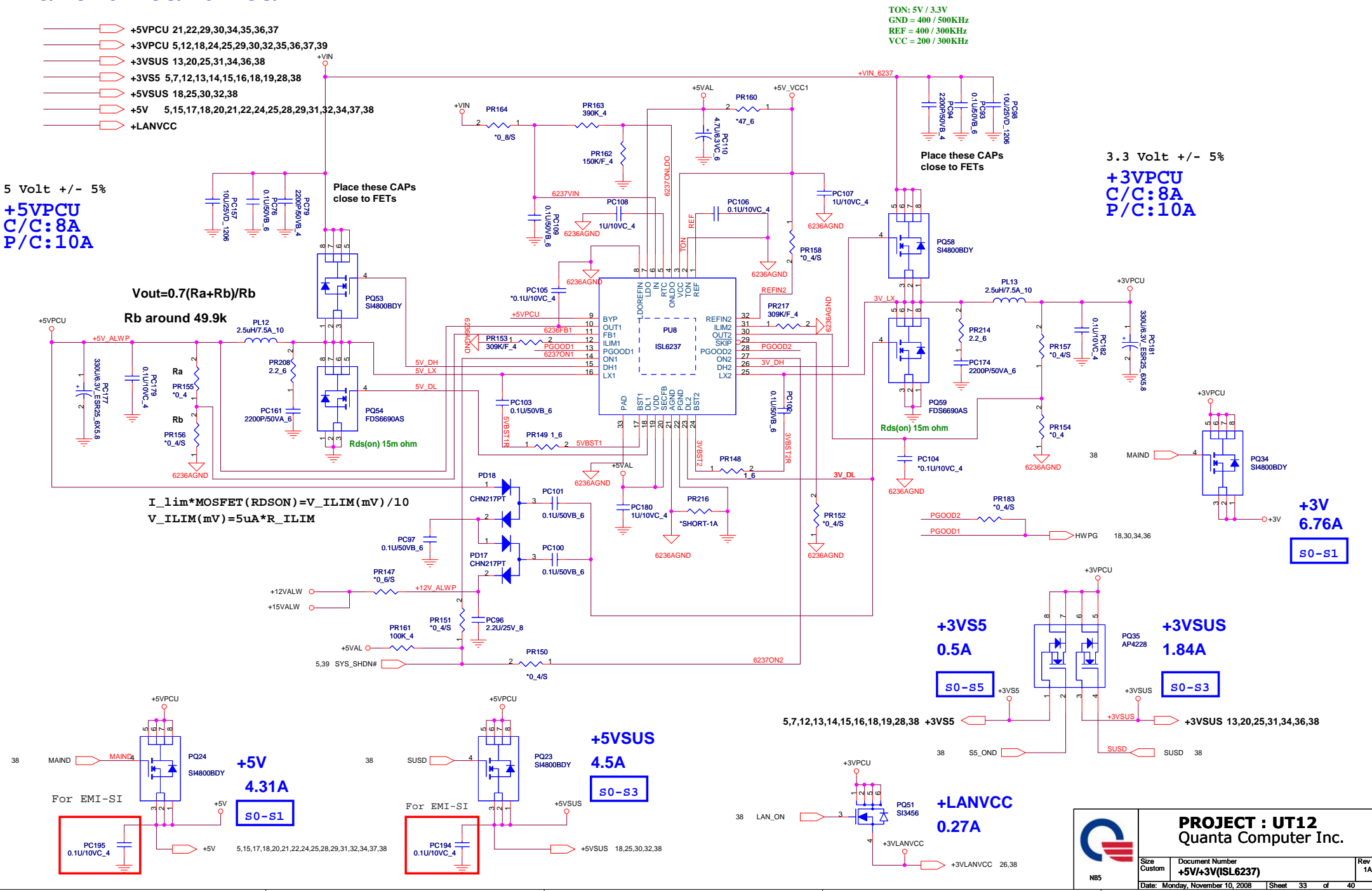




## Mini PCI-E Card 2 TV tuner card









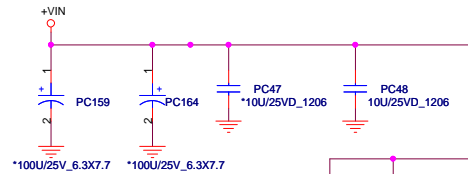
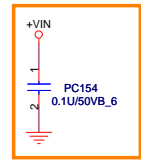
DYN_PWR_EN	High	Low
<b>+1.1V_DYN</b>	<b>1.0</b>	<b>1.1</b>



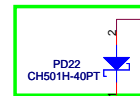
**WWW.AliSaler.Com**

+2.5V 3  
+1.8VSUS 3,4,5,6,7,35,37

EC:SI(11/07)

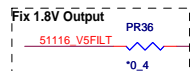
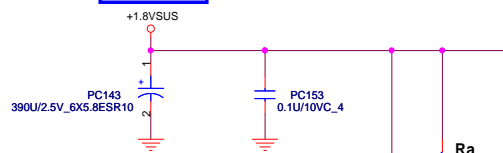


EC:SI(11/07)

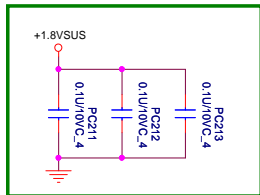


$I_{lim(Valley)} = 10\mu A * R_{ILIM} / R_{DS\_ON}$   
For OCP set.

23.65A  
S0~S3



Add 0.1u CAP PC211, PC212, PC213 for EMI

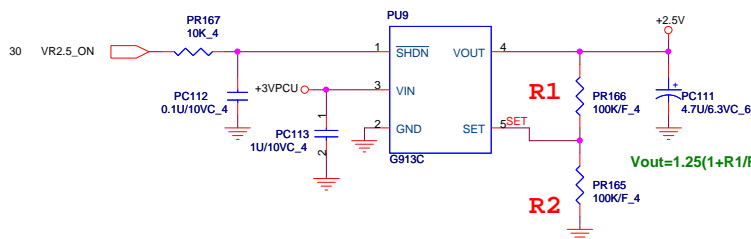


$R_a = (V_{out} - 0.75) / 0.75 * R_b$   
Rb value from 100K to 300K ohm

+2.5V  
0.25A  
S0~S1

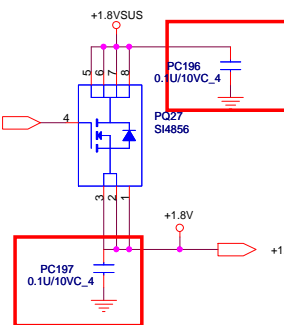
S0~S1

Close to CPU  
SI power



$V_{out} = 1.25 * (1 + R1/R2)$

For EMI-SI



Discrete:SI4856  
UMA:SI4800

For EMI-SI

+1.8V  
10.4A  
S0~S1

S0~S1

Mode	Discharge Mode
V5IN	No discharge
VDDQ	Tracking discharge
Gnd	Non-tracking discharge

$V_{TRIP}(mV) = R_{TRIP}(Kohm) * 10(\mu A)$

$I_{OCP} = V_{trip} / R_{ds\_on} + I_{Ripple} / 2$

VDDQSET	VDDQ(V)	VTTREF and Vtt	Note
GND	2.5	$V_{\_vddqsns} / 2$	DDR
V5IN	1.8	$V_{\_vddqsns} / 2$	DDR2
FB	adjustable	$V_{\_VDDQSNS} / 2$	$1.5V < VDDQ < 3V$

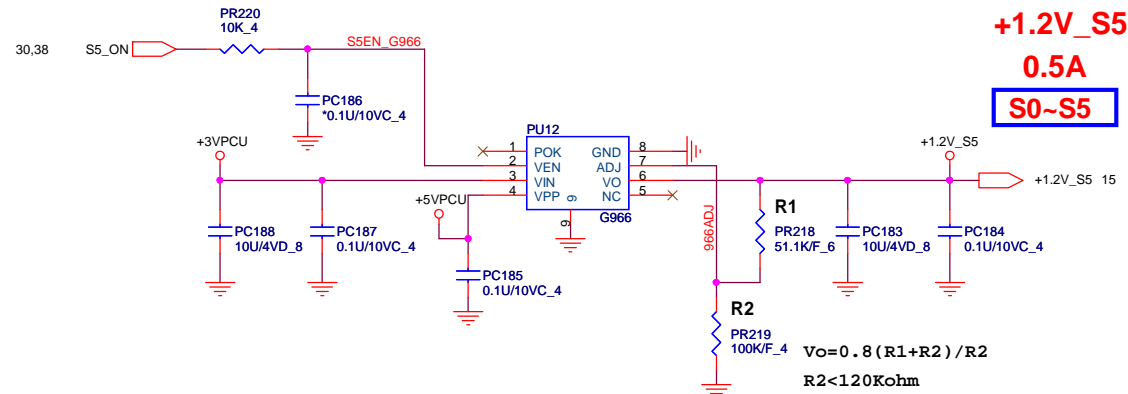
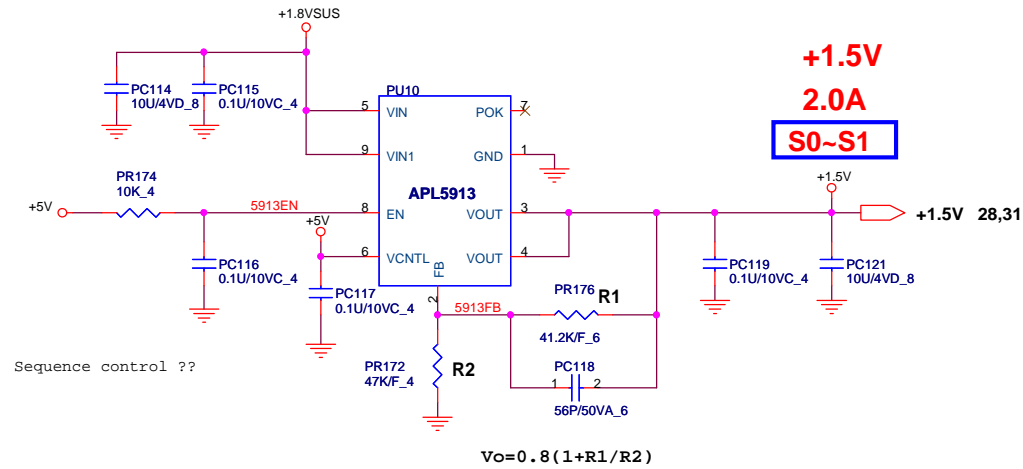
PROJECT : UT12  
Quanta Computer Inc.

Size Custom

Document Number 1.8VSUS/DDR\_VTER/+1.8V/2.5V

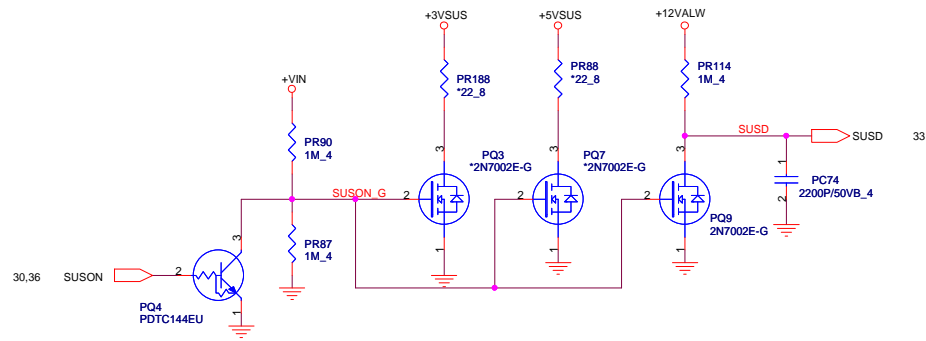
Date: Monday, November 10, 2008 Sheet 36 of 40

Rev 1A

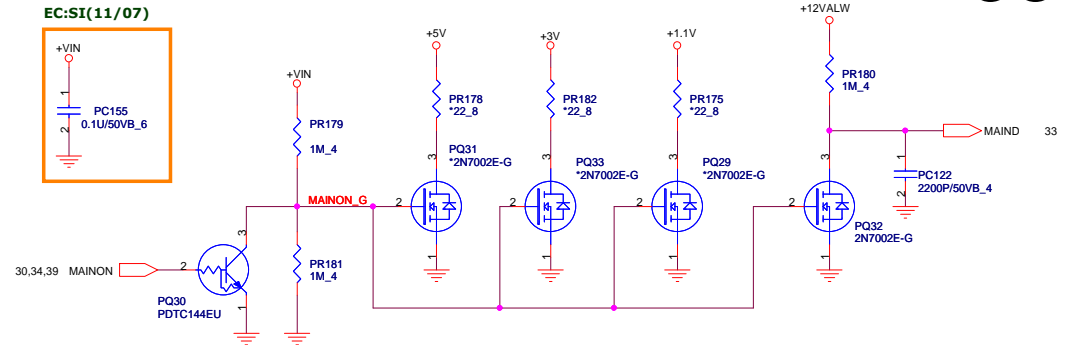
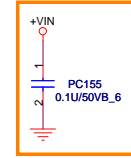


**PROJECT : UT12**  
**Quanta Computer Inc.**

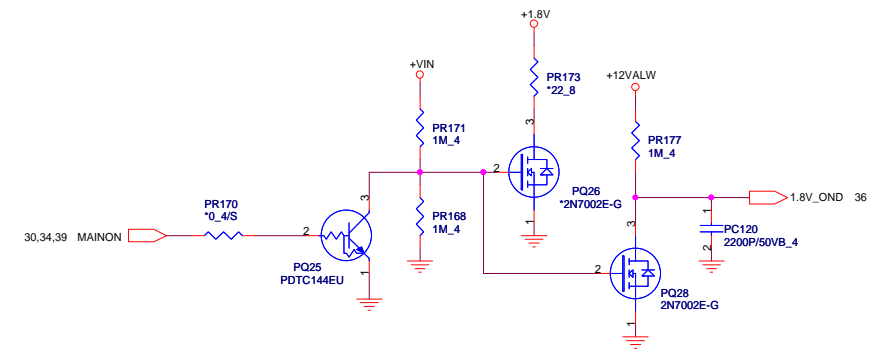
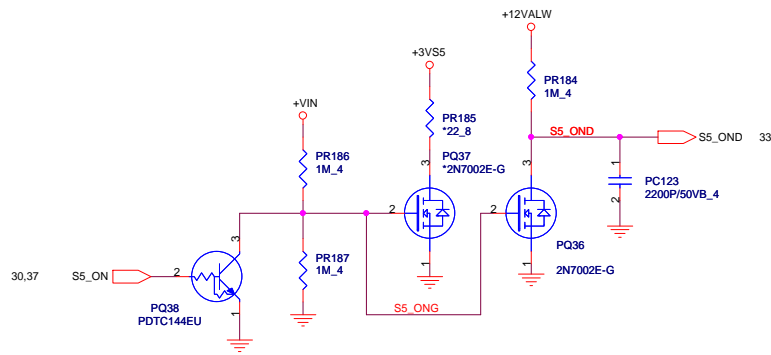
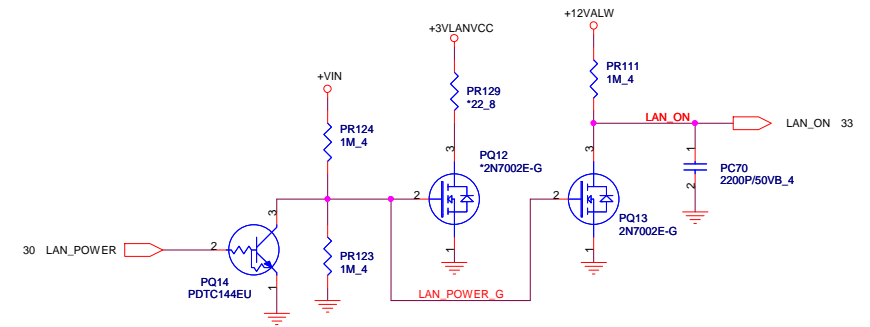
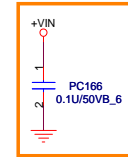
Size B	Document Number <b>VGA PWR OZ8118/1.2V_S5/+1.5</b>	Rev 1A
Date: Monday, November 10, 2008 Sheet 37 of 40		



EC:SI(11/07)



EC:SI(11/07)



**PROJECT : UT12**  
Quanta Computer Inc.

Size Custom	Document Number <b>DISCHARGE</b>	Rev 1A
Date: Monday, November 10, 2008	Sheet 38 of 40	

